Evening Panel
International Symposium on FPGAs, 2009

CMOS vs. NANO
Comrades or Rivals?

Monterey, California
February 23, 2009

Co-chairs
Deming Chen
Russell Tessier
Technology trend

2007 ITRS Product Technology Trends - Half-Pitch, Gate-Length

- Before 1998 .71X/3YR
- After 1998 .71X/2YR
- MPU M1 .71X/2.5YR
- MPU & DRAM M1 & Flash Poly .71X/3YR
- Flash Poly .71X/2YR
- Nanotechnology (<100nm) Era Begins -1999
- Gate Length .71X/3YR
- GLpr IS = 1.6818 x GLph

Year of Production

2007 - 2022 ITRS Range
How low can we go?

- Future devices could theoretically scale down to
  - 1.5 nm
  - with 0.04 ps switching speeds
  - and 0.017 electron volts in terms of power consumption.

Can CMOS get there?

- **Process challenges:** manufacturing solutions beyond 22nm are not known
- **Power challenges:**
- **Reliability challenges:**
- Others: random doping variations, short channel effects, surface scattering …

C. Hu, et al., IEDM, 2000

D. Barlage, et al., MRS, 2006
Alternatives

- nanowires
- carbon nanotubes
- graphene
- III-V-based chips
- spintronics
- phase change logic devices
- interference devices
- optical switches
- ...
Case Study 1: nanowire (NW)

- High-density nanowire crossbar memory
- High-density logic
- High-density routing

The pitch of the NWs can be much smaller than lithographic patterning, using a bottom-up self-assembly process.


A. DeHon, et al., FPGA, 2004

G. Snider et al., Nanotechnology, 2007
Case Study 2: carbon nanotube (CNT)

- CNT device on delay and energy×delay product.

- CNT bundle interconnect on delay and thermal conductance.


Carbon nanotube (cont’)

- CNT-based nanoFPGA offers high density and high performance

C. Dong, et al., FPGA, 2009
But, unsolved issues for NANO remain

- **High defect rate**
  - In the HP crossbar memory, only 85% of the switches can switch, where 50% of these ‘good’ switches can only switch once.

- **Variation beyond photolithography**
  - Mixture of metallic and semiconducting CNTs
  - Distribution of CNT diameters

- **Fabrication challenges**
  - Difficulty of fine-grained positioning of the CNTs
  - Problematic interface between CNT and contact

- “It can be done on a lab scale, but we don't know how to put millions of them on a wafer.”
  - Mike Mayberry, VP, technology manufacturing group, Intel.
So, what will be the future of CMOS and NANO?

Are they
A. Comrades?
B. Rivals?
C. Strangers?
D. Too early to say?
Best Picture from OSCAR 2009: "Slumdog Millionaire"
Experts in the panel

- Prof. Kaustav Banerjee  
  - University of California, Santa Barbara
- Dr. Mojy C. Chian  
  - Technology Development, Altera
- Prof. André DeHon  
  - University of Pennsylvania
- Dr. Shinobu Fujita  
  - Corporate R&D Center, Toshiba
- Dr. James Hutchby  
  - Semiconductor Research Corporation (SRC)
- Dr. Steve Trimberger  
  - Xilinx Research Labs, Xilinx
Detailed discussion items

- Does NANO offer new capabilities that are sufficiently compelling for investment and learning?
- What impact, if any, will bottom-up fabrication have?
- What are the pros and cons of the CMOS/Nano hybrid solution?
- How will FPGAs fare in this disruption (if any) compared to others? Will it upset the balance of power?
- Do nanoscale issues force architectural changes and paradigm shifts? What are the trends? Who will be impacted?
- Will FPGA vendors take the lead in this new paradigm and opportunity?
Panel: CMOS vs. Nano: Comrades or Rivals?

Kaustav Banerjee

University of California, Santa Barbara
Major Challenges in CMOS/FPGA

- Power consumption
- Interconnection
- Process variation
Power Consumption in FPGAs

Xilinx Virtex II
Dynamic power breakdown

Xilinx Spartan-3
Leakage power breakdown
Tuan et al., *CICC*. 2003

Interconnect: 60%
Logic: 26%
Clocking: 14%

Interconnect: 38%
Configuration SRAM Cells: 34%
LUTs: 16%
Other: 12%
So, What Can Be Done?

Nanotechnologies offer potential solutions...
Carbon Based Interconnect Materials

Carbon Nanotubes
Mono-layer Graphene Nano-Ribbon
Multi-layer Graphene Nano-Ribbon
CNT vs. Cu Interconnects

**Performance**
Li et al., TED 2009 (in press)

**Power Dissipation**
Srivastava et al., TNT 2009 (in press)

**Thermal/Reliability**
Srivastava et al., IEDM 2005

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**Delay Ratio w.r.t Cu**
- d-GNR ($p=0.41$)
- d-GNR ($p=1$)
- SWCNT ($F_m=1$)
- SWCNT ($F_m=1/3$)
- DWCNT ($D=1.5\text{nm}$)
- MWCNT ($D=14\text{nm}$)

**Min. Interconnect Width**
- 22 nm
- 18 nm
- 14 nm

**Total Buffer Width**
(times minimum)

---

K. Banerjee, UCSB

PANEL: FPGA’09, February 22–24, 2009, Monterey, CA
CNT Interconnect Fabrication...

[Kreupl et. al., (Infineon) *IEDM*, 2004]

[Sato et. al., (Fujitsu) IITC, 2006]

[Awano et al., (Fujitsu) 2006]

[Choi et. al., (Samsung) Nano Conf., 2006]

[Nihei et. al., (Fujitsu) IITC, 2007]
Integration with Cu/Low-k Dielectric

CNT Single Kelvin via grown at 400 °C

A. Kawabata et. al., IITC, 2008

CNT via is robust under current high-density stress over long time.....
Leakage Increases with Scaling
Sub-threshold Slope Engineering

\[ S = \left( \frac{d[\log(I_d)]}{dV_g} \right)^{-1} = \left( 1 + \frac{C_{dm}}{C_{ox}} \right) \frac{kT}{q} \ln 10 \]

Subthreshold swing (mV/decade)

An ideal switch

Solid-state devices

\[ S = \Delta V_{gs}/\Delta \log(I_d) \]

\[ \Delta V_{gs} \]

\[ V_{th} \]

Gate voltage (V_{gs})

Drain current (log(I_d))

\[ \Delta \log(I_d) \]

\[ Dadvgour et al., DAC 2007 \]

NEM-FET, NWFET, Fe-FET

TFET, IMOS

Dadgour et al., DAC 2007
Conclusions

CMOS: mature and experienced

Emerging nano-technologies: energetic but inexperienced

CMOS still rules!

Hybrid technologies…way to go!

K. Banerjee, UCSB

PANEL: FPGA’09, February 22–24, 2009, Monterey, CA
Inflection Point for FPGA

Mojy C. Chian
VP, Technology
Altera Corp
Feb ‘09
Scaling: The Good, Bad and Ugly

- **Good:**
  - Higher density
  - Higher performance & throughput
  - More features & functionality
  - Lower power per function
  - Lower cost per function

- **Bad and Ugly:**
  - Higher development cost development
  - Higher unit cost (wafer)
  - Increasing complexity
  - Increasing variability
  - Higher total power (for fixed die size)
ITRS Performance Scaling

From 2008 ITRS Update

- Introduction of multigate transistor (MuGFET) delayed to 2015
- Lgate scaling slowing to ~0.71x every 3.8 years
- Intrinsic speed increase of ~13% per year, down from ~17% per year
The Ideal Routing Switch

“Ideal” Routing Switch Attributes

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<tr>
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<th>Value</th>
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<td>Non-volatile</td>
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<td>Number of Terminals</td>
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<td>On Resistance</td>
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<td>Off Resistance</td>
<td>&gt; 1E9 Ohms</td>
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<tr>
<td>Program/Erase Time</td>
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<tr>
<td>Program Current</td>
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<tr>
<td>Program Voltage</td>
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<tr>
<td>Erase Voltage</td>
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<td>Operating Temp Range</td>
<td>From -40 C to 125 C</td>
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<tr>
<td>Lifetime</td>
<td>10 years</td>
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<tr>
<td>Placement of switches</td>
<td>No restriction</td>
</tr>
<tr>
<td>SEU</td>
<td>no SEU</td>
</tr>
<tr>
<td>on/off cycles</td>
<td>&gt; 10,000</td>
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<tr>
<td>Availability</td>
<td>Lead process node</td>
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</table>

- Lower Vcc and higher leakage pose increasing challenges for implementing FPGA routing switch.
- Replacement of routing pass gate could enable significant performance/power benefit.

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Process Technology: Friend or Foe?

- Adopting advanced process technologies
  Increased complexity and slow down in benefits?

- But ........

We have opportunities ahead like never before
Estimated Development Costs Complex ASSP SoC Designs

Millions $

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<tr>
<th>Technology</th>
<th>Design, Test, Verification</th>
<th>Embedded Software</th>
<th>Mask</th>
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Gartner

Semiconductor Industry Update October 2008
Chip Development Business Model

- **Cost:**
  - Development cost: NRE
  - Unit cost: COGS

- **FPGA versus ASIC/ASSP:**
  - Trade off of NRE and COGS
  - Low volume: emphasis on NRE reduction
  - High Volume: emphasis on COGS reduction

- **Reality check – an example:**
  - R&D = $100M
  - Market Share = 20%
  - ASP = $20
  - R&D = 20% of revenue
  - → **TAM = $2.5B** (there are not too many markets of this size)
  - Many low volume ASIC/ASSP providers have a broken business model
    - The financial model is not sustainable
    - The situation is exasperated with increased R&D cost for newer technologies
## ASIC % Design Starts by Technology

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**Total** | 100    | 100    | 100    | 100    | 100    | 100    | 100    | 100    | 100    | 100    | 100 |

#1 ASIC Design Technology

Source: Altera & Gartner

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### Key Points
- **#1 ASIC Design Technology**: FPGA
- **#1 PLD Design Technology**: FPGA

**Source**: Altera & Gartner

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Average ASIC Density

Note: Data based on Gartner Dataquest

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FPGA to Full ASIC Path

- Solution points in NRE – Unit Cost Space
  - Rationalized volume forecast is the key to strategy

Unit Cost

- **FPGA**
- **Hardened FPGA**
  - FPGA companion base die with 5 masks programmable
- **Re-Packaged FPGA**
  - FPGA Companion die in a smaller package
- **Full ASIC**
Summary

- Significant challenges exist for technology scaling
  - We are in the era of power-constrained scaling
  - Variability will continue to increase
- Innovations expected to enable continued scaling
  - HKMG, MuGFETs, high-mobility channels, …
- But they increase complexity and cost
- Bifurcation in ASIC/ASSP offerings
  - Only a small portion can afford adopting advanced technologies

This is all music for FPGA

- The most significant opportunities for FPGA is in share gain from ASIC & ASSP
- Advanced process technologies are tipping the scale in favor of FPGA
- We are at an inflection point
CMOS vs. Nano
FPGA2009 Panel

André DeHon
andre@seas.upenn.edu
Position

1. Beneficial to work with nature (physics).
2. Atomic-scale is noisy and statistical.
3. Fine-grained reconfiguration and continuous adaptation are powerful.
4. Regularity is good.
5. Randomness can be harnessed for good.
6. Lithographic CMOS is the new PCB.
Beneficial to work with nature

• …rather than against it.

• Atomic-scale offer:
  – New switching/communication phenomena
  – New ways to define structures, dimensions, and spacing
  – New ways to perform assembly
Beneficial to work with nature

See: http://www.dna.caltech.edu/Papers/DNAorigami-nature.pdf for some wonderful images of DNA Assembly and details on how to perform the assembly.

• Deeper understanding atomic-scale physics
  – Increases our palette → better solutions
    • Favorable E,D,A tradeoffs, cheaper manufacture
Beneficial to work with nature

• …but today, we are stumbling our through it like clumsy, ignorant giants
Atomic-scale is noisy and statistical.

- The **nature** of atomic-scale elements is statistical.
  - ➔ anything we build at this scale
    - Lithographic or bottom up
  - ....will behave statistically
    - kT, uncertainty principle, tunneling, ....

- Will lead to
  - Defects, Variation, Misbehavior

- Current approaches are brute force attempts to **hide** this nature
  - Millions of electrons, thousands of dopants, large noise margins.

...work with nature not against it.
Fine-Grained Reconfiguration

• Selecting devices → role mapping after fabrication is powerful.
  – Mitigation fabrication statistics
    • Defects
    • Variation
  – Mitigate lifetime changes

• FPGA-like architectures have a potential head-start over alternatives.
Regularity

• Regular structures easier to self-assemble
  – Low information content
  – Exploit natural phenomena

• E.g.
  – Large area 50 nm period grating by multiple nanoimprint lithography and spatial frequency doubling. B Cui, Z Yu, H Ge, and SY Chou, APPLIED PHYSICS LETTERS, 90, 043118 (2007)

• FPGA-like architectures exploit regularity
  – While providing diversity for computation
Randomness

• Can be a tool for good
  – Diversity creation
  – Expanders (LDPCs, network routing)
  – CAD
  – Randomized Algorithms
  – Heavily exploited by nature
    • …work with nature.
CMOS is the new PCB

- Differential Reliability
  - Islands of stability & determinism
    - diagnose, supervise, configure
- Lithographic CMOS does this well
- Provides the substrate on which atomic-scale things can be assembled
- **Goal:** reliability of CMOS with \{E,D,A\} of atomic-scale building blocks
  - Compare DRAM memories
1. Beneficial to work with nature.
2. Atomic-scale is noisy and statistical.
3. Fine-grained reconfiguration and continuous adaptation are powerful.
4. Regularity is good.
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6. Lithographic CMOS is the new PCB.
Nano-electronics for Near-Future FPGA

Shinobu Fujita

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R&D of Nano-electronics and their Applications
FPGA needs something other than CMOS scaling for future?

FPGA cannot replace ASIC enough.. (Power, Area, Speed..)

Source: iSuppli

TOSHIBA Leading Innovation
FPGA vs ASIC after CMOS ending

CMOS FPGA

CMOS ASIC

Current Near Future Future

32nm CMOS 22nm CMOS 16nm CMOS

65nm CMOS 45nm CMOS 32nm CMOS

Ending...
Cost(/Performance) is too bad..
Gap between current FPGA and Future Nano-electronics?

Current FPGA Architecture

- CMOS (65nm, 40nm, 32nm..)
- NAND-flash ROM
- Cost increase makes CMOS ending..

Nano Architecture

- New Post-Si Transistor
- New Post-Si Technologies (non-volatile memory)

Current Time gap…

Dilemma...

Current FPGA Architecture Nano Architecture

S. Fujita, International Symposium on FPGA ’09
Solutions for Near Future FPGA!

Current FPGA Architecture
- CMOS (65nm, 40nm, 32nm..)
- NAND-flash ROM

Near Future
- New non-volatile Memories (PRAM, FeRAM, MRAM, ReRAM, mature process)

Future
- Nanowire-FET
- New Post-Si Technologies (non-volatile memory)

Cons:
- Very High Parasitic Resistance…

S. Fujita, International Symposium on FPGA ’09
Segregated dopants at the S/D interface efficiently reduce Schottky barrier height.

- **Low Source/Drain resistance**
  (Superior performance of PASS Transistor logic!!)
- **Short channel effect immunity**
- **Enhanced carrier injection velocity**

(A. Kinoshita et al, (Toshiba), IEDM 2006)
CMOS-Ex for FPGA
Dopant Segregated Schottky (DSS) MOSFETs

Superior performance of PASS Transistor logic!!
Also, CMOS performance is superior to conventional one.

(T. Kinoshita et al, (Toshiba), IEDM 2006)

S. Fujita, International Symposium on FPGA ’09
Pass Tr. Logic (FPGA)

\[ V_{\text{out}} = \text{Low} \rightarrow \text{High} \]

\[ V_{s-d} \approx \frac{1}{4} V_{\text{out}} \]

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Higher current at lower Vsd (DSS-MOSFET)
New-nonvolatile Memories for FPGA

W. Wong et al, (Stanford, Toshiba) IEDM 2006

TiOx based RAM

On/Off  R ratio > 10^7

SRAM-based configuration

Non-Volatile-RAM-based

Reduce Power & Area
Requirement to NV-RAM for replacing config-SRAM

- High off-Resistance (to reduce leakage current)  
  \(<100\text{pA, } = 1\text{V}/10\text{Gohm!}) \ @100\times100\text{nm}^2\)
- High On/Off ratio …. At least \(>100\), or \(>10^6\)
- Programming voltage: higher than Vdd of CMOS
- Long-term retention: \(>10\text{years}\)
- Long-term reliability: NO memory disturbance during logic operation
- Plus.. decreasing programming current

*Different requirements from those for memory circuits!*
Conclusion
Solutions for Near Future FPGA!

Current FPGA Architecture

- CMOS (65nm, 40nm, 32nm..)
- NAND-flash ROM

Near Future

- CMOS-Ex DSS-FET
- New non-volatile Memories

Future

- New Post-Si Transistor
- New Post-Si Technologies (non-volatile memory)

Important Bridge between Two

Thank you!
(mature process)

S. Fujita, International Symposium on FPGA ’09
FPGA ‘09 Evening Panel
CMOS vs. Nano: Comrades or Rivals?

CMOS Extension and “Beyond CMOS”
Information Processing Technologies

February 23, 2009

Jim Hutchby - SRC
FPGA ‘09 Evening Panel
CMOS vs. Nano: *Neither - They are Family*

CMOS Extension and “Beyond CMOS”
Information Processing Technologies

February 23, 2009

Jim Hutchby - SRC
FPGA ‘09 Evening Panel
CMOS IS NANO

CMOS Extension and “Beyond CMOS”
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Jim Hutchby - SRC
CMOS IS NANO

- Critical dimension < 100nm
  - Gate length & Channel thickness
- New physics for nano device
  - Quantum confinement in channel
End of the Road map??

NO!

Geometrical Scaling  ➔  Functional Scaling
The Reign of CMOS Continues – Geometrical Scaling will Shift to Functional Scaling

- ITRS ERD & ERM are evaluating devices and technologies to extend CMOS to and beyond 2024
- ITRS ERD & ERM are looking for novel solutions for information processing for applications beyond 2024
  - Integrated with CMOS platform
  - Eventually stand alone
- Heterogeneous integration of diverse functions (e.g., NEMS, Sensors, Analog, RF, Bioelectronics, etc.) in “Functional Diversification” is changing technology requirements for integrated electronics.
# 2007 High Performance Logic Roadmap
Illustrating Need for New High-velocity Channel Materials

<table>
<thead>
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</thead>
<tbody>
<tr>
<td>DRAM ½ Pitch (nm) (contacted)</td>
<td>65</td>
<td>57</td>
<td>50</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>22</td>
<td>20</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td></td>
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</tr>
<tr>
<td>MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)</td>
<td>68</td>
<td>59</td>
<td>52</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>22</td>
<td>20</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td></td>
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<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>25</td>
<td>22</td>
<td>20</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td>13</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lg: Physical Lgate for High Performance logic (nm) [1]</td>
<td>25</td>
<td>22</td>
<td>20</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td>13</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5.5</td>
<td>5</td>
<td>4.5</td>
</tr>
<tr>
<td>Effective Ballistic Enhancement Factor , Kbal [12]</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Extended Planar Bulk</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<td></td>
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<tr>
<td>UTB FD</td>
<td>1.05</td>
<td>1.1</td>
<td>1.16</td>
<td>1.2</td>
<td>1.24</td>
<td>1.28</td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DG</td>
<td>1.17</td>
<td>1.25</td>
<td>1.31</td>
<td>1.37</td>
<td>1.53</td>
<td>1.67</td>
<td>1.87</td>
<td>1.99</td>
<td>1.97</td>
<td>2.11</td>
<td>2.11</td>
<td>2.11</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

Ultimate CMOS scaling needs new channel materials with enhanced ballistic velocity.
2007/08 - PIDS/FEP - Simplified Transistor Roadmap

[Examples of “Equivalent Scaling” from ITRS PIDS/FEP TWGs]

Electrostatic control

- poly SION
- bulk
- PDSOI
- stressors
- + substrate engineering

Gate stack

- metal high k
- FDSOI
- + high µ SiGe materials
- 3D
- MuGFET MuCFET

[ITRS DRAM/MPU Half-Pitch Timing:

- 65nm 2007/7.5
- 45nm 2010
- 32nm 2013
- 22nm 2016
- 16nm 2019]

Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

Work in Progress – Do Not Publish
Alternate Channel Materials and Structures for Extending CMOS

Alternate channel materials and structures for extending CMOS beyond silicon & III-V compound semiconductors include:

- Nanowires,
- Nanotubes, and
- Graphene
Nanotube FET

Band gap: $0.5 - 1 \text{ eV}$
On-off ratio: $\sim 10^6$
Mobility: $\sim 100,000 \text{ cm}^2/\text{Vsec} @\text{RT}$
Ballistic @RT: $\sim 300-500 \text{ nm}$
Fermi velocity: $10^6 \text{ m/sec} (V_F)$
Max current density: $> 10^9 \text{ A/cm}^2$

Schottky barrier switching

## Nanowire & Single Electron Transistors

![Diagram of Nanowire Transistor]

<table>
<thead>
<tr>
<th></th>
<th>Nanowire FET</th>
<th>SET</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Channel</strong></td>
<td>1-dimensional</td>
<td>Island/quantum dot</td>
</tr>
<tr>
<td><strong>Channel length</strong></td>
<td>5 – 10nm</td>
<td>1 – 10nm(^1)</td>
</tr>
<tr>
<td><strong>Capacitance</strong></td>
<td>aF</td>
<td>aF</td>
</tr>
<tr>
<td><strong>Conductance</strong></td>
<td>Channel resistance or electron-injection limited 10 – 100mS</td>
<td>Tunnel-limited 0.02 – 2mS</td>
</tr>
<tr>
<td><strong>Gain</strong></td>
<td>High/marginal</td>
<td>Low(^2)</td>
</tr>
<tr>
<td><strong>ON/OFF state</strong></td>
<td>Single</td>
<td>Multiple</td>
</tr>
</tbody>
</table>

\(^1\) Assuming quantum dot width\n
\(^2\) Assumes multiple for SET
How low can we go?

- Future devices could theoretically scale down to
  - 1.5 nm
  - with 0.04 ps switching speeds
  - and 0.017 electron volts in terms of power consumption.

CMOS scaling on track to obtain physical limits for electron devices

George Bourianoff / Intel

Bolzmann-Heisenberg Limit

$3k_B T \ln 2$

$10^4 k_B T$

$500 k_B T$

$3k_B T \ln 2$
Graphene Electronics: Conventional & Non-conventional

Conventional Devices

FET

Band gap engineered Graphene nanoribbons

Graphene quantum dot

(Manchester group)

Nonconventional Devices

Graphene Veselago lens

Cheianov et al. Science (07)

Graphene Spintronics

Son et al. Nature (07)

Graphene pseudospintronics

Trauzettel et al. Nature Phys. (07)
Spin FET

Schematic Spin gain FET structure with a MnGe/SiGe quantum well.

JingJing Chen and KL Wang et al., App. Phys. Letts. 90, 012501 2007
Supplementing CMOS

A possible ultimate evolution of on-chip architectures is Asynchronous Heterogeneous Multi-Core with Hierarchical Processors Organization.

General Purpose Processor

Basis of Existing Assessments of Logic Devices

Courtesy Fawzi Behmann - Freescale
Top down information processing
Image Recognition

Tadashi Shibata, University of Tokyo
# Image recognition

## TABLE I

**PERFORMANCES COMPARISON OF IMAGE RECOGNITION SYSTEMS**

Search target: Sella (a pituitary gland)  
Number of templates (generated by learning algorithm): 15  
Search Area: 75x100-pel area

<table>
<thead>
<tr>
<th></th>
<th>Power (W)</th>
<th>Computational time (Second)</th>
<th>Total energy (J)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pentium 4 1.5GHz</td>
<td>54.7</td>
<td>5</td>
<td>273.5</td>
</tr>
<tr>
<td>Optimized in an assembly language level</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mobile Pentium 3 500MHz/1.1V</td>
<td>3.5</td>
<td>15</td>
<td>52</td>
</tr>
<tr>
<td>Optimized in an assembly language level</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Our digital vector generator &amp; neural analog associative processor</td>
<td>0.152</td>
<td>1.2</td>
<td>0.182</td>
</tr>
</tbody>
</table>

*Tadashi Shibata, University of Tokyo*
Summary

- Geometrical and functional scaling is projected by the ITRS into the 2020’s and likely beyond.
  - New MOSFET device structures are available
  - New “Channel Replacement” materials are being explored
  - Combinations of new materials & new structures are being investigated.

- Several new “Beyond CMOS” switching phenomena and “State Variables” are being pursued for new information processing approaches
  - No approach has been shown as a clear winner
  - Carbon-based Nanoelectronics has significant potential

- New markets requiring Functional Diversification will become important technology driver
CMOS vs. Nano: No contest.

Steve Trimberger

Safe-Harbor Statement: This document contains forward-looking statements. Opinions expressed in this presentation are my own and do not necessarily reflect the opinion of my employer or my employer’s marketing department.

“Next week I plan to think about the option of using technology that isn’t yet available.”
- Wally in Dilbert 2007. Scott Adams
## Engineering Fiction

<table>
<thead>
<tr>
<th>Action</th>
<th>Science Fiction</th>
<th>Engineering Fiction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cite a new effect or technology</td>
<td>Radiation induces mutation</td>
<td>Carbon nanotubes</td>
</tr>
<tr>
<td>Ignore limitations</td>
<td>Mutations can cause creatures to grow to enormous size</td>
<td>Scale up to manufacturability: quality, reproducibility</td>
</tr>
<tr>
<td>Postulate an infrastructure around it</td>
<td>Large creatures can survive unnoticed under the oceans</td>
<td>Nano fabrication facilities</td>
</tr>
<tr>
<td>Cite real, unimpeachable data</td>
<td>Dinosaurs had thick skin</td>
<td>Design a NAND gate from CNT switches</td>
</tr>
<tr>
<td>Tell fanciful stories</td>
<td><em>Godzilla!</em></td>
<td><em>Nano-scale FPGA!</em></td>
</tr>
</tbody>
</table>
Why CMOS for FPGAs today?
Questions to the Panel

1) Do atomically-engineered materials and fabrication techniques offer new capabilities that are sufficiently compelling to encourage the necessary investment and learning?
   – Yes, better is better.

2) What impact, if any, will bottom-up fabrication have---augment lithographic processes, replace lithography, or remain a lab curiosity?
   – Despite problems with optical lithography (see next slide), any displacing technology will need to give superior quality and reliability. You will know they’re getting serious when they talk about purification techniques.
Lithography History & Future

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2) What impact, if any, will bottom-up fabrication have—augment lithographic processes, replace lithography, or remain a lab curiosity?
   – Despite problems with optical lithography, any displacing technology will need to give superior quality and reliability. You will know they’re getting serious when they talk about purification techniques.

3) What are the pros and cons of the CMOS/Nano hybrid solution?
   – Cost effective: only apply new technology where needed.
Questions to the Panel

4) How will FPGAs fare in this disruption (if any) compared to alternatives (ASICs, processors, multi/many-cores)? Will it upset the balance of power (Intel, Xilinx, Altera, HP, WindRiver, XtremeData, startups)?
   – Fabrication technology won’t change the balance of power, unless only one player can get it. Nano is so difficult that it is likely it requires the entire industry to produce it. Then all will have it.

5) Do nanoscale issues force architectural changes and paradigm shifts? What are the trends? Who will be impacted (FPGA designers, FPGA CAD, FPGA users)?
   – Circuits may change. No change to the model is required. “We do Deep Sub-Micron design, so you don’t have to” If necessary, we’ll do Nano, so you don’t have to.

6) Will FPGA vendors take the lead in this new paradigm and opportunity? Or, are they so risk-averse that they will leave it to startups?
   – No. FPGA vendors are too smart to take the lead. Notice that they don’t take the lead in process development or computer development today.
- Nano might work
 Nano might work someday.
 But we are WAY too early.
 And there’s plenty to do right now that will benefit our customers.