Evening Panel

International Symposium on FPGAs, 2009

CMOS vs. NANO

Comrades or Rivals?

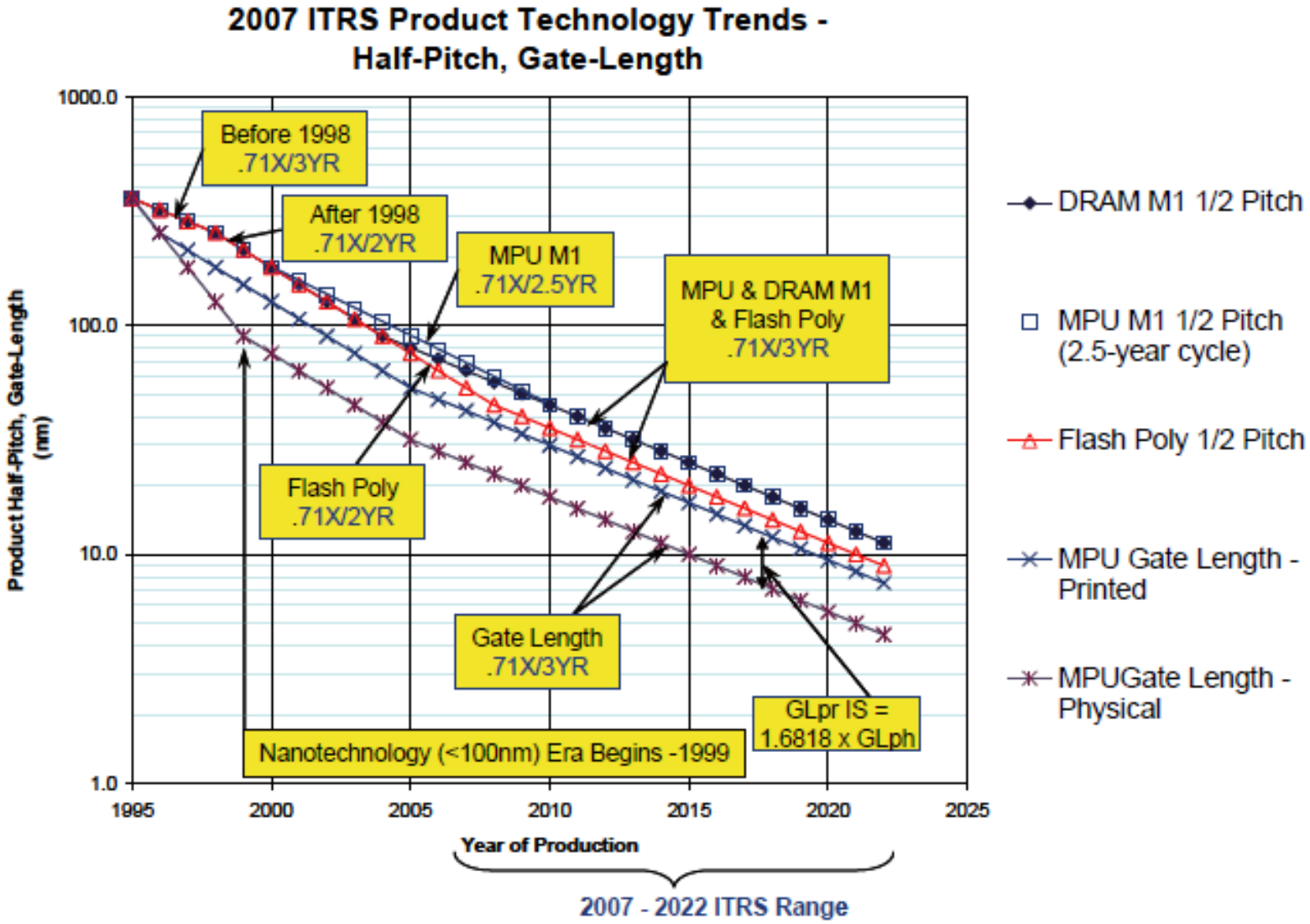
Monterey, California
February 23, 2009

Co-chairs

Deming Chen

Russell Tessier

Technology trend



How low can we go?

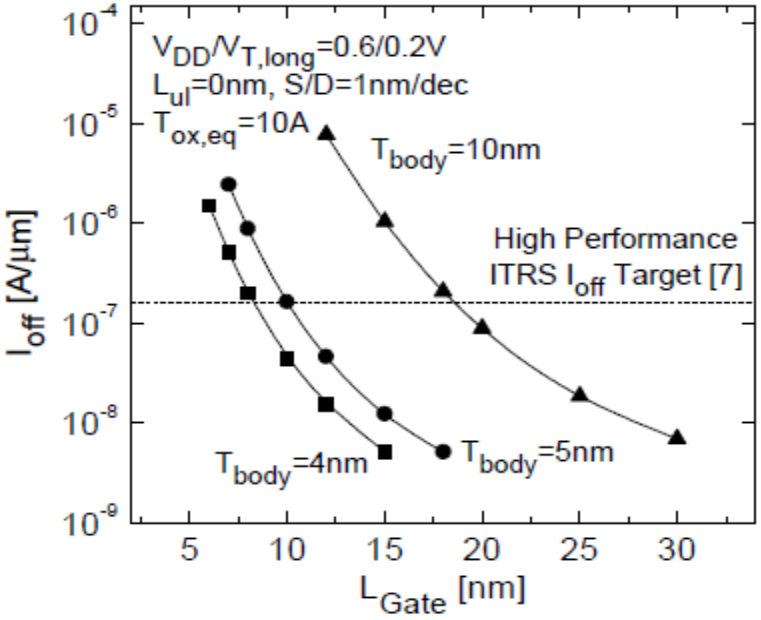
- Future devices could theoretically scale down to
  - 1.5 nm
  - with 0.04 ps switching speeds
  - and 0.017 electron volts in terms of power consumption.

J. Hutchby, G. Bourianoff, et al., *Proc. of IEEE*, 2003

Can CMOS get there?

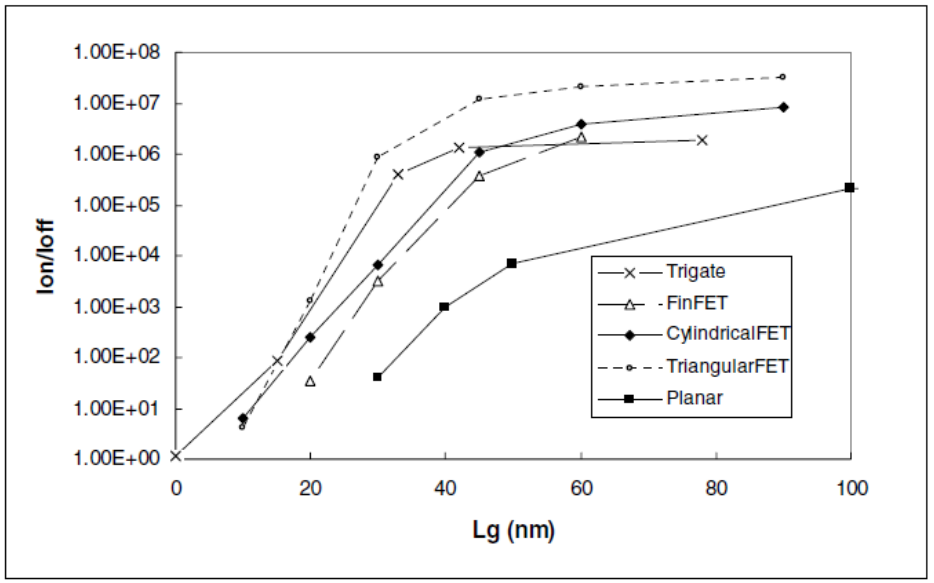
- **Process challenges: manufacturing solutions beyond 22nm are not known**

- **Power challenges:**



C. Hu, et al., *IEDM*, 2000

- **Reliability challenges:**



D. Barlage, et al., *MRS*, 2006

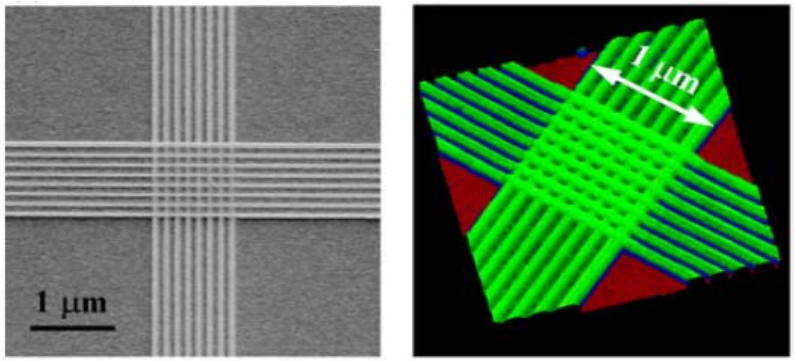
- **Others: random doping variations, short channel effects, surface scattering …**

Alternatives

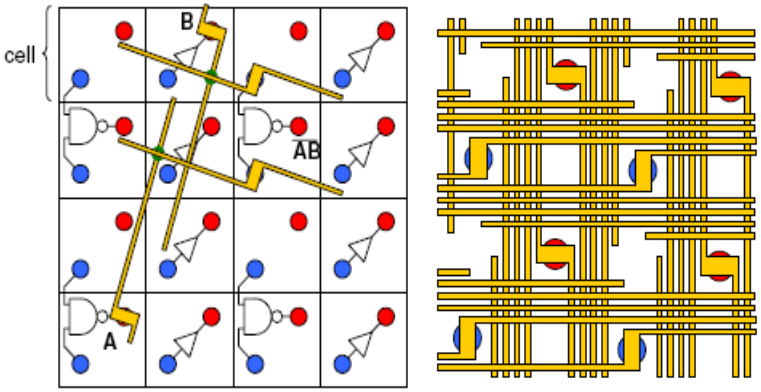
- nanowires
- carbon nanotubes
- graphene
- III-V-based chips
- spintronics
- phase change logic devices
- interference devices
- optical switches
- …

Case Study 1: nanowire (NW)

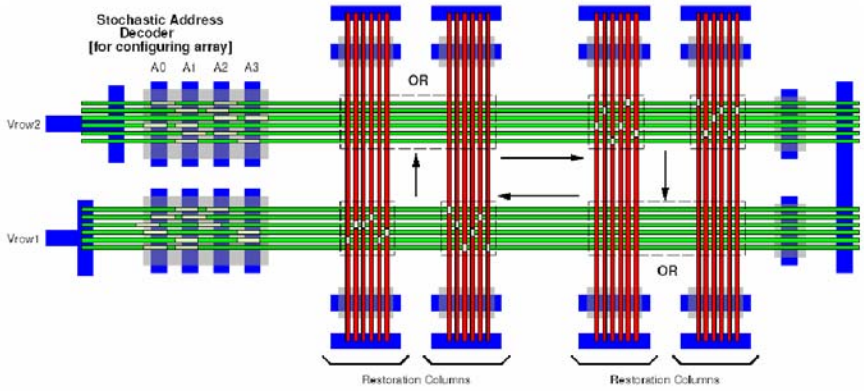
- High-density nanowire crossbar memory
- High-density logic
- High-density routing



Y. Chen, et al. *Nanotechnology*, 2003



G. Snider et al., *Nanotechnology*, 2007

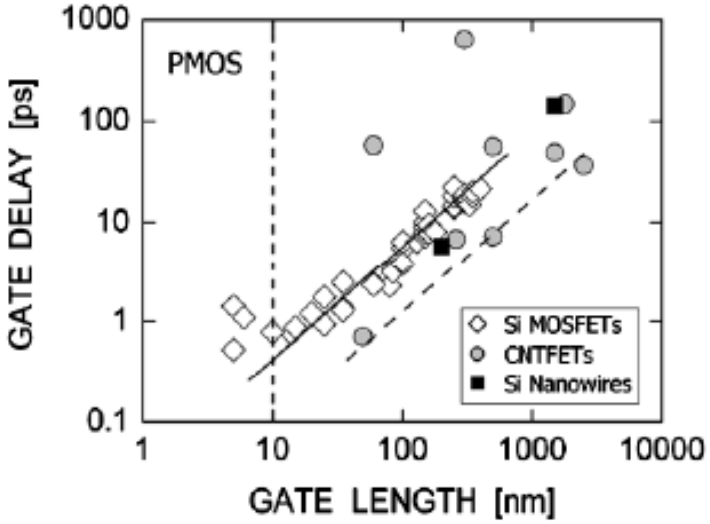


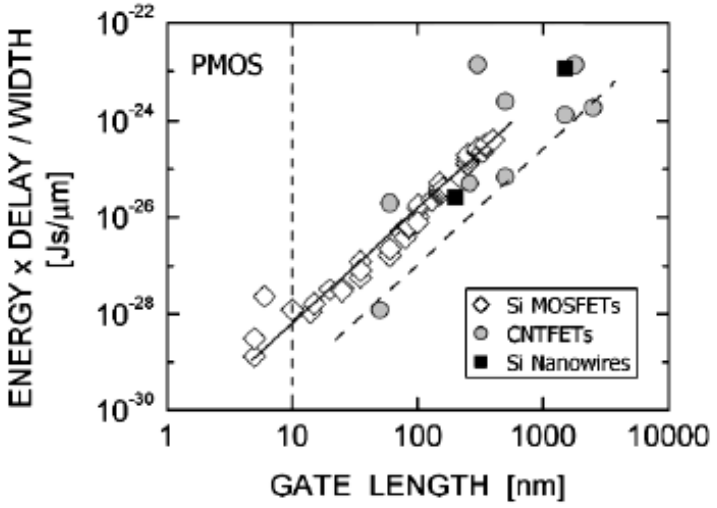
A. DeHon, et al., *FPGA*, 2004

The pitch of the NWs can be much smaller than lithographic patterning, using a bottom-up self-assembly process

Case Study 2: carbon nanotube (CNT)

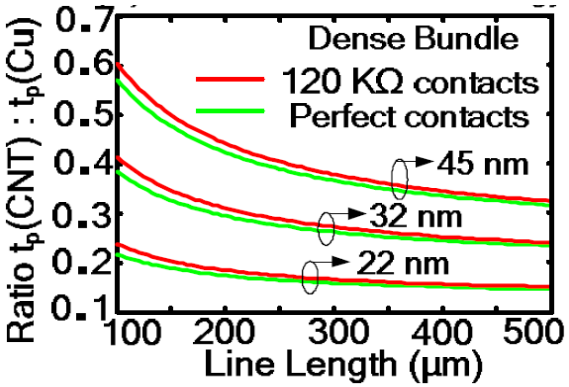
- CNT device on delay and energy×delay product.

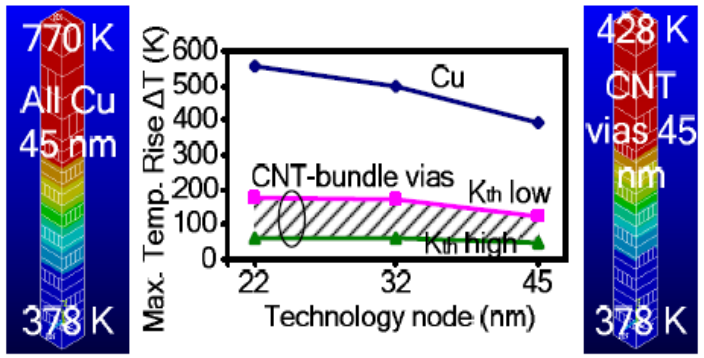




R. Chau, et al., *Trans. Nano.*, 2005

- CNT bundle interconnect on delay and thermal conductance.

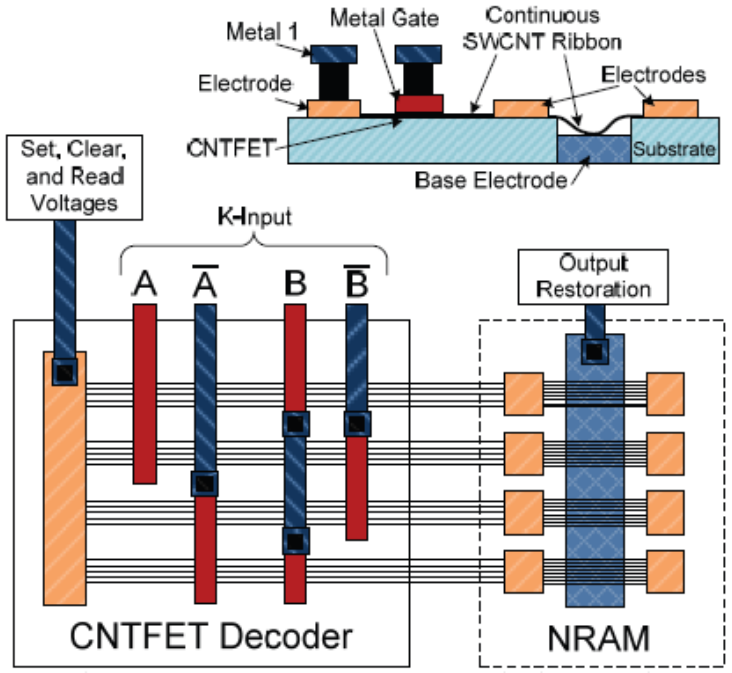




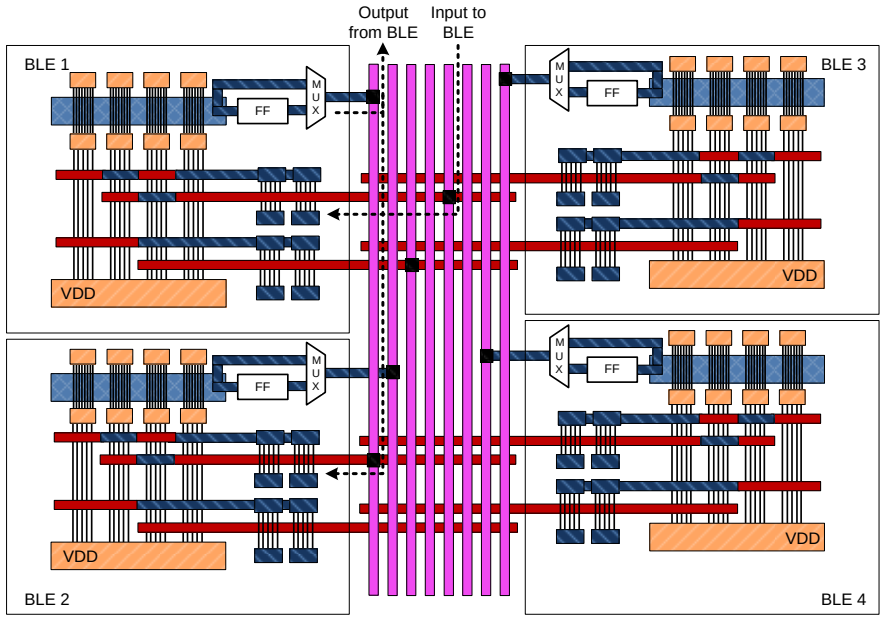
N. Srivastava, K. Banerjee, *IEDM,* 2005

Carbon nanotube (cont')

- CNT-based nanoFPGA offers high density and high performance



LUT design



CLB design

C. Dong, et al., *FPGA,* 2009

But, unsolved issues for NANO remain

- High defect rate
  - In the HP crossbar memory, only 85% of the switches can switch, where 50% of these ‘good’ switches can only switch once.
- Variation beyond photolithography
  - Mixture of metallic and semiconducting CNTs
  - Distribution of CNT diameters
- Fabrication challenges
  - Difficulty of fine-grained positioning of the CNTs
  - Problematic interface between CNT and contact

- “It can be done on a lab scale, but we don't know how to put millions of them on a wafer.”
  - Mike Mayberry, VP, technology manufacturing group, Intel.

So, what will be the future of CMOS and NANO?

Are they

A. Comrades?
B. Rivals?
C. Strangers?
D. Too early to say?

Best Picture from OSCAR 2009: "Slumdog Millionaire"

Experts in the panel

- Prof. Kaustav Banerjee
  - University of California, Santa Barbara
- Dr. Mojy C. Chian
  - Technology Development, Altera
- Prof. André DeHon
  - University of Pennsylvania
- Dr. Shinobu Fujita
  - Corporate R&D Center, Toshiba
- Dr. James Hutchby
  - Semiconductor Research Corporation (SRC)
- Dr. Steve Trimberger
  - Xilinx Research Labs, Xilinx

Detailed discussion items

- Does NANO offer new capabilities that are sufficiently compelling for investment and learning?
- What impact, if any, will bottom-up fabrication have?
- What are the pros and cons of the CMOS/Nano hybrid solution?
- How will FPGAs fare in this disruption (if any) compared to others? Will it upset the balance of power?
- Do nanoscale issues force architectural changes and paradigm shifts? What are the trends? Who will be impacted?
- Will FPGA vendors take the lead in this new paradigm and opportunity?

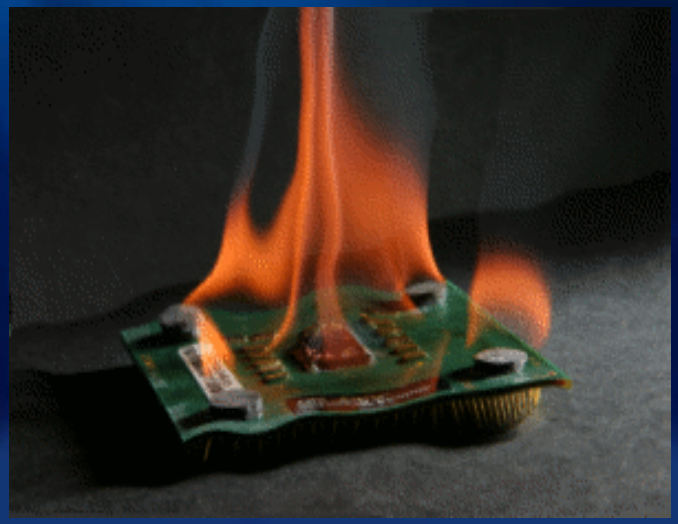
FPGA'09, February 22–24, 2009, Monterey, CA

Panel: CMOS vs. Nano: Comrades or Rivals?

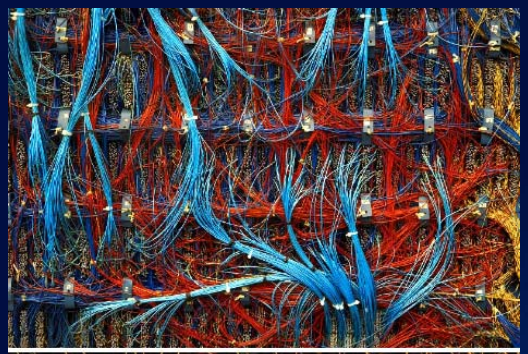
Kaustav Banerjee

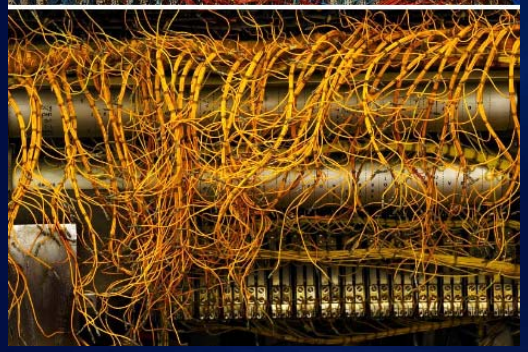
University of California, Santa Barbara

Major Challenges in CMOS/FPGA



Power consumption

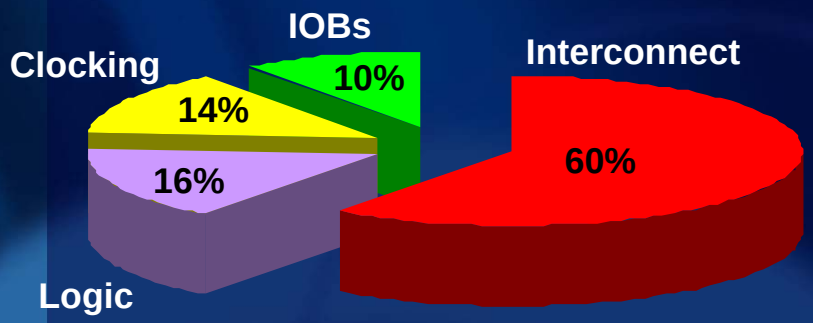




Interconnection

Process variation

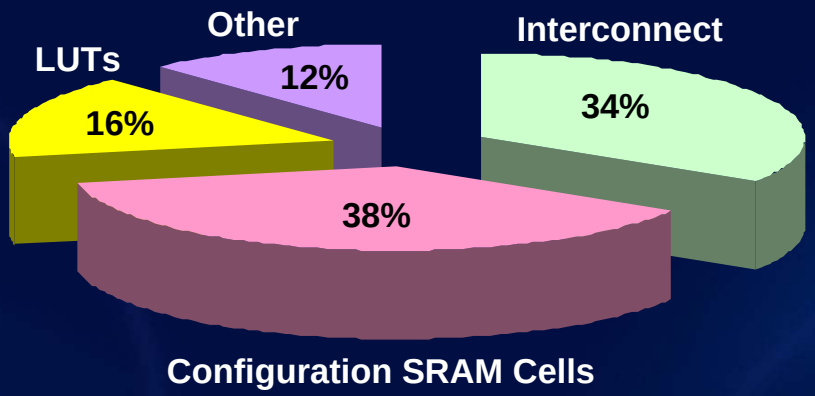
Power Consumption in FPGAs



Xilinx Virtex II

Dynamic power breakdown

Shang, et al. *FPGA. 2002*

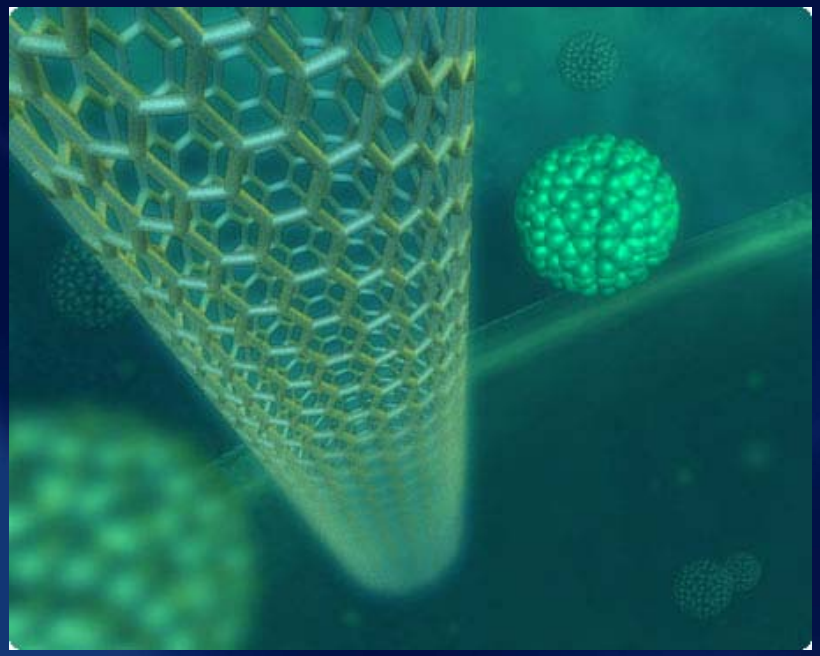


Xilinx Spartan-3

Leakage power breakdown

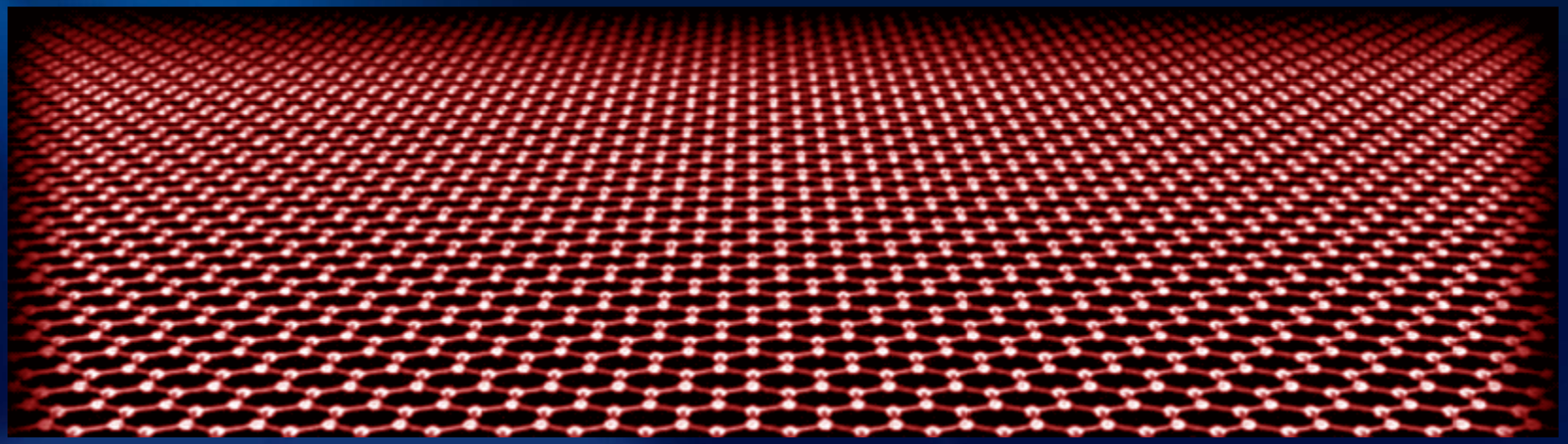
Tuan et al., *CICC. 2003*

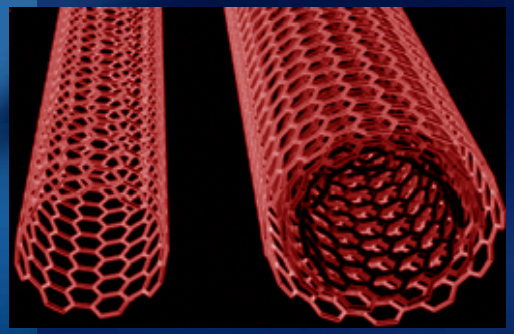
So, What Can Be Done?



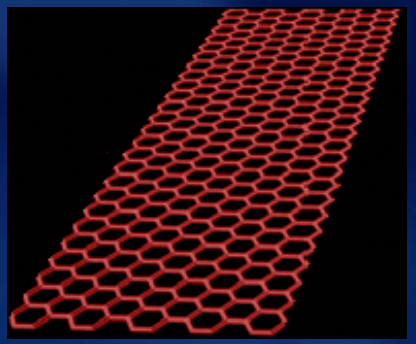
- **Nanotechnologies offer potential solutions…**

Carbon Based Interconnect Materials

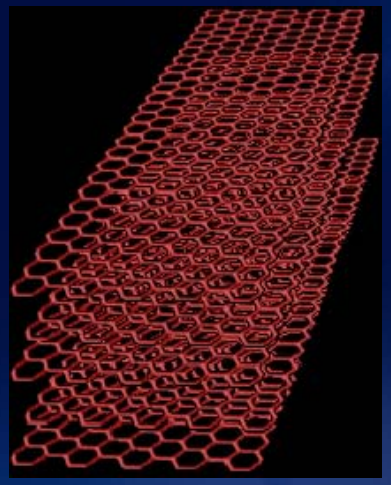




Carbon Nanotubes

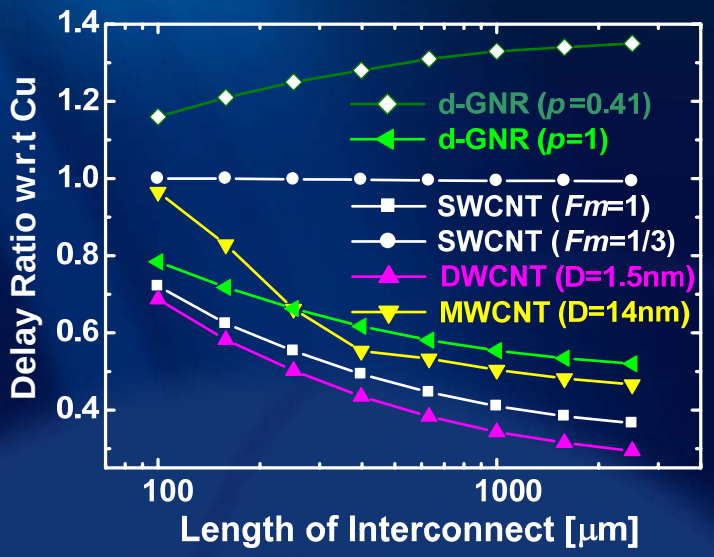


Mono-layer Graphene Nano-Ribbon

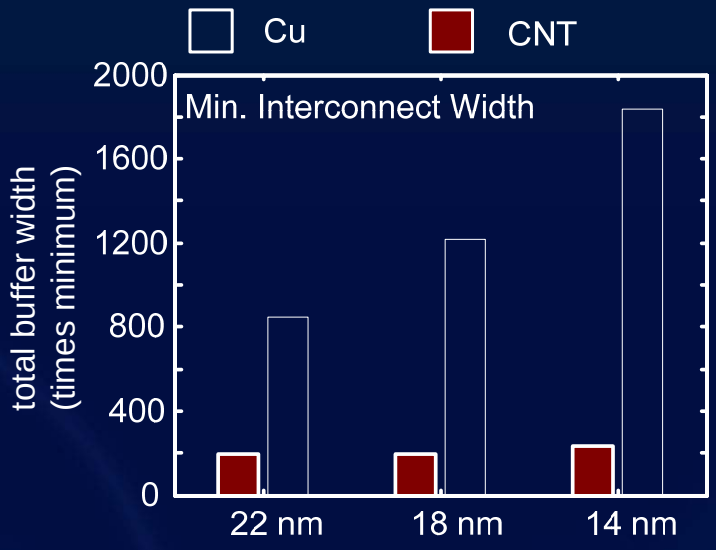


Multi-layer Graphene Nano-Ribbon

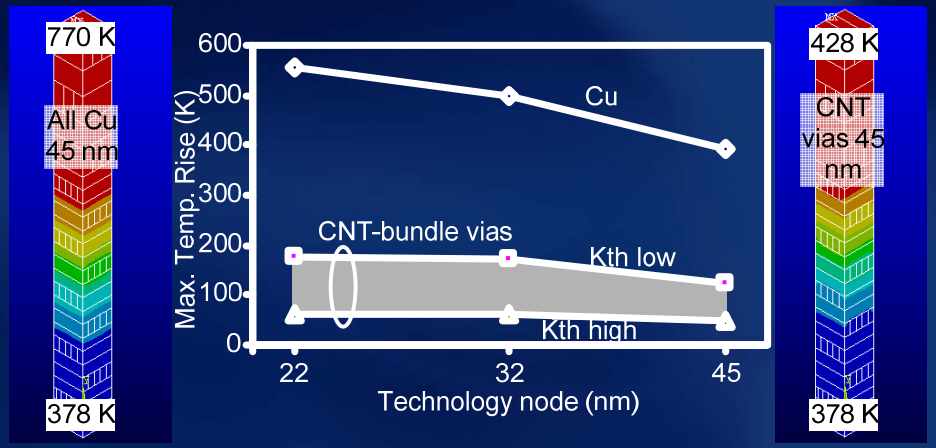
CNT vs. Cu Interconnects



Performance
Li et al., TED 2009 (in press)

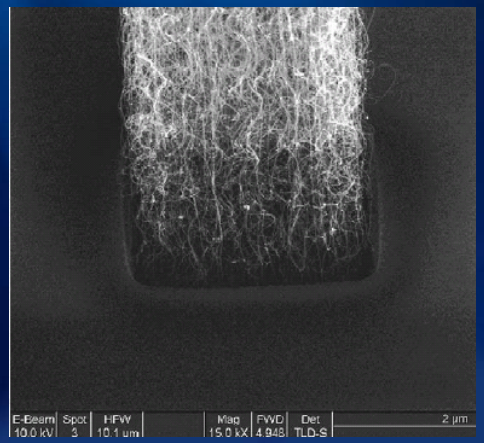


Power Dissipation
Srivastava et al., TNT 2009 (in press)

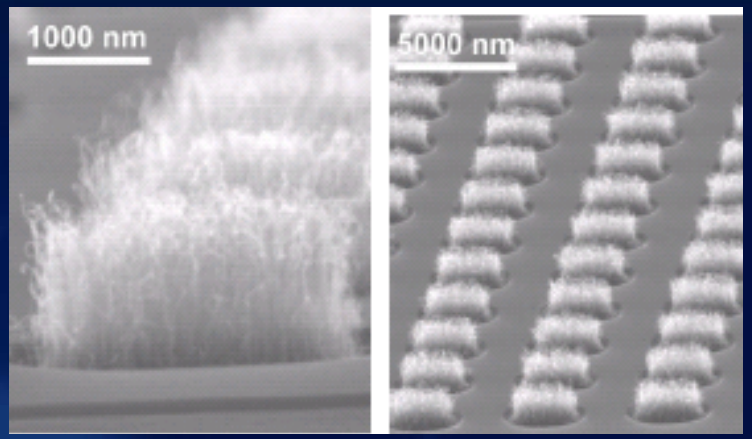


Thermal/Reliability
Srivastava et al., IEDM 2005

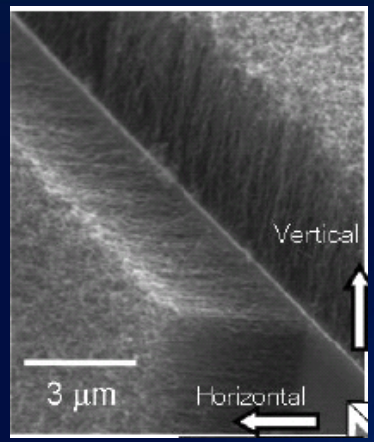
CNT Interconnect Fabrication…



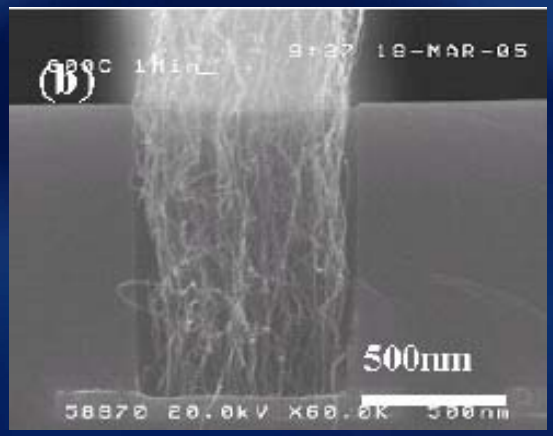
[Kreupl et. al., (Infineon) *IEDM*, 2004]



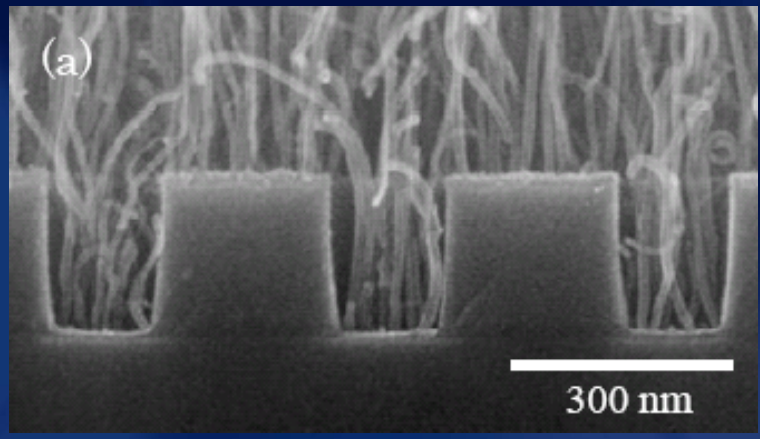
[Sato et. al., (Fujitsu) IITC, 2006]



[Awano et al., (Fujitsu) 2006]



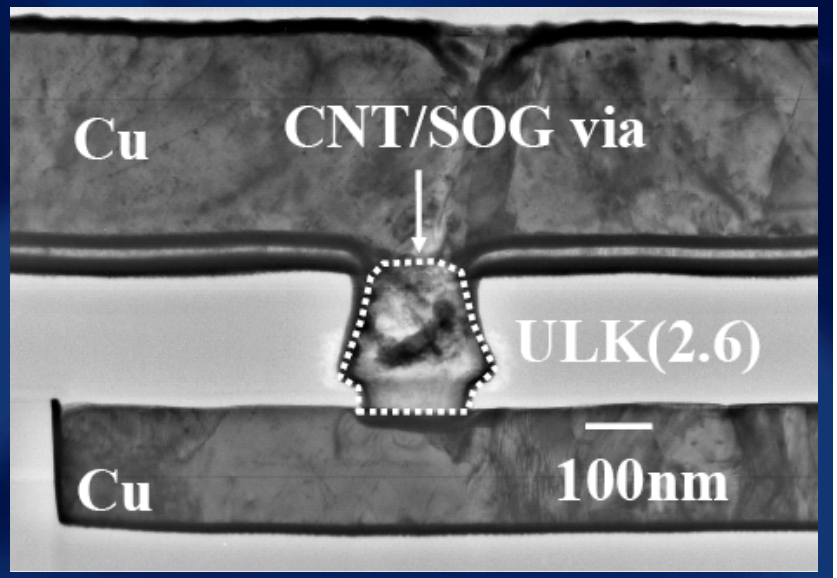
[Choi et. al., (Samsung) Nano Conf., 2006]

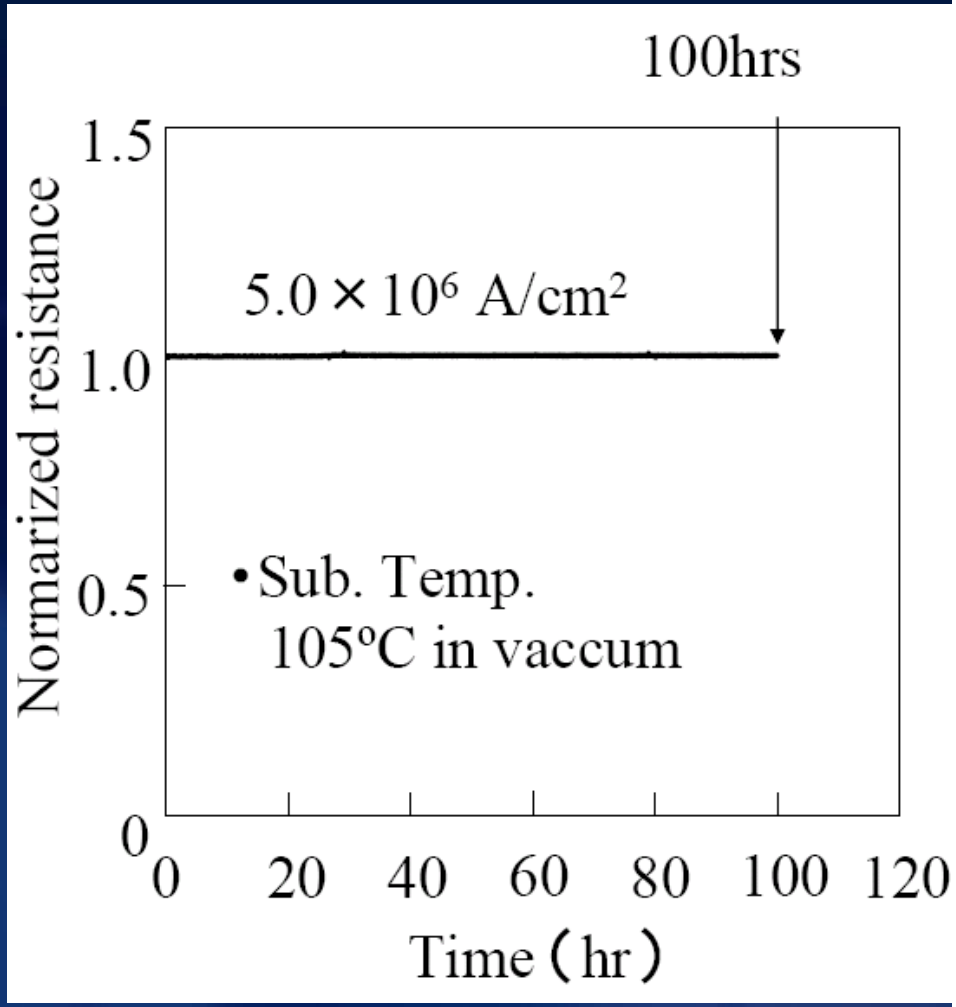


[Nihei et. al., (Fujitsu) IITC, 2007]

Integration with Cu/Low-k Dielectric

CNT Single Kelvin via grown at 400 ^{0}C

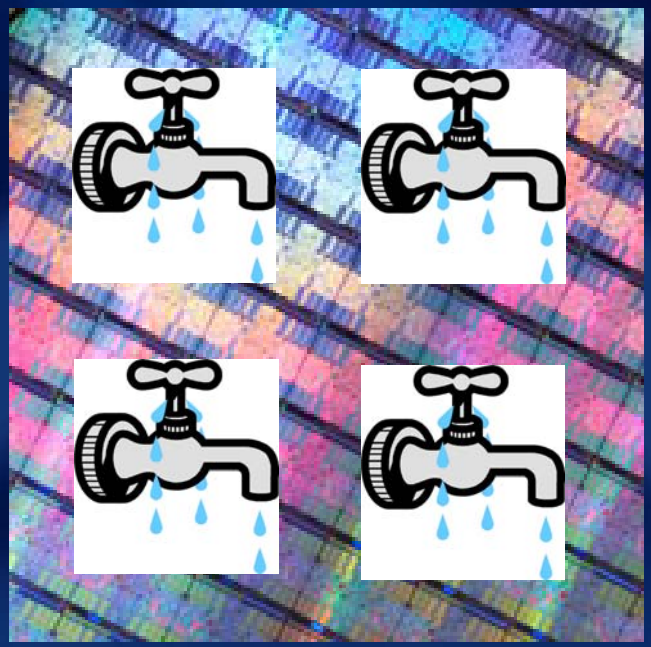




A. Kawabata et. al., *IITC*, 2008

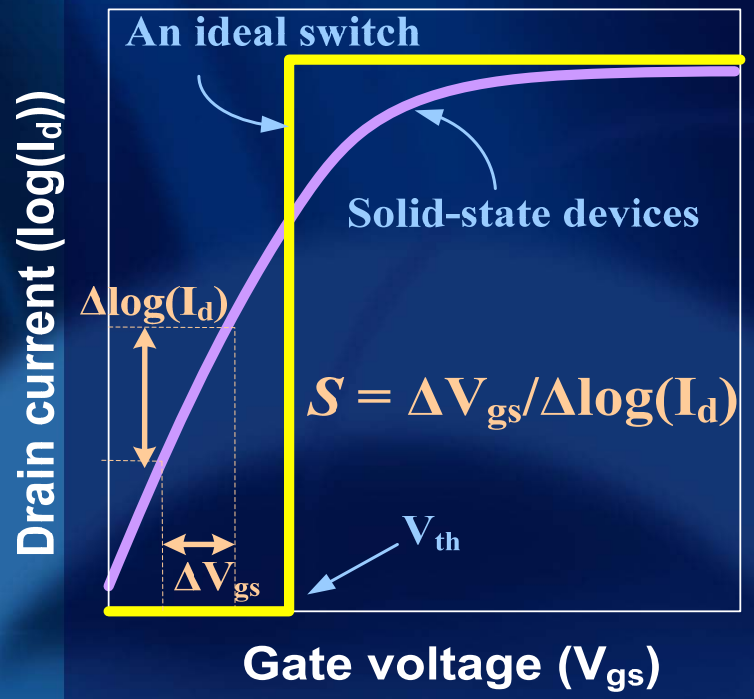
CNT via is robust under current high-density stress over long time.....

Leakage Increases with Scaling



Device Scaling

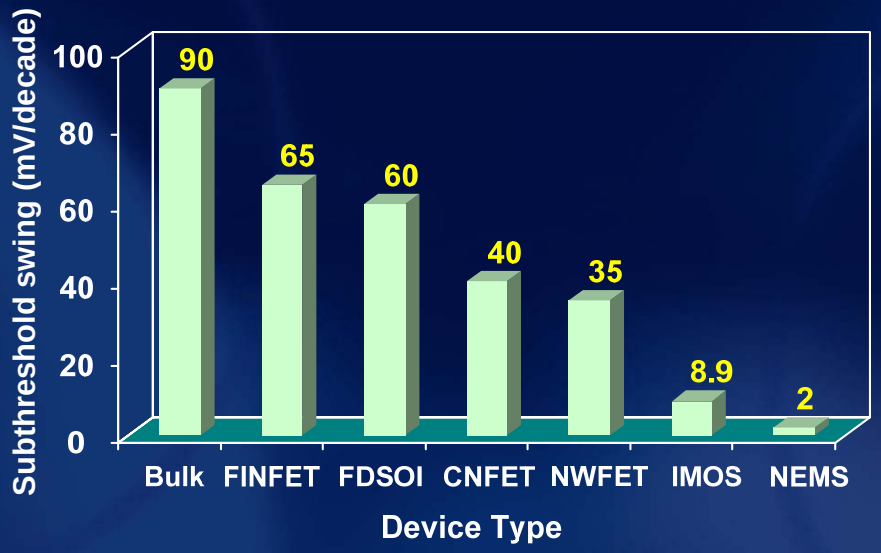
Sub-threshold Slope Engineering



$$S = \left(\frac{d[\log I_d]}{dV_g} \right)^{-1} = \left(1 + \frac{C_{dm}}{C_{ox}} \right) \frac{kT}{q} \ln 10$$

NEM-FET, NWFET, Fe-FET

TFET, IMOS



Dadgour et al., *DAC 2007*

Conclusions

CMOS: mature and experienced

CMOS still rules!

Emerging nano-technologies: energetic but inexperienced

Hybrid technologies….way to go!

Inflection Point for FPGA

Mojy C. Chian
VP, Technology
Altera Corp
Feb '09

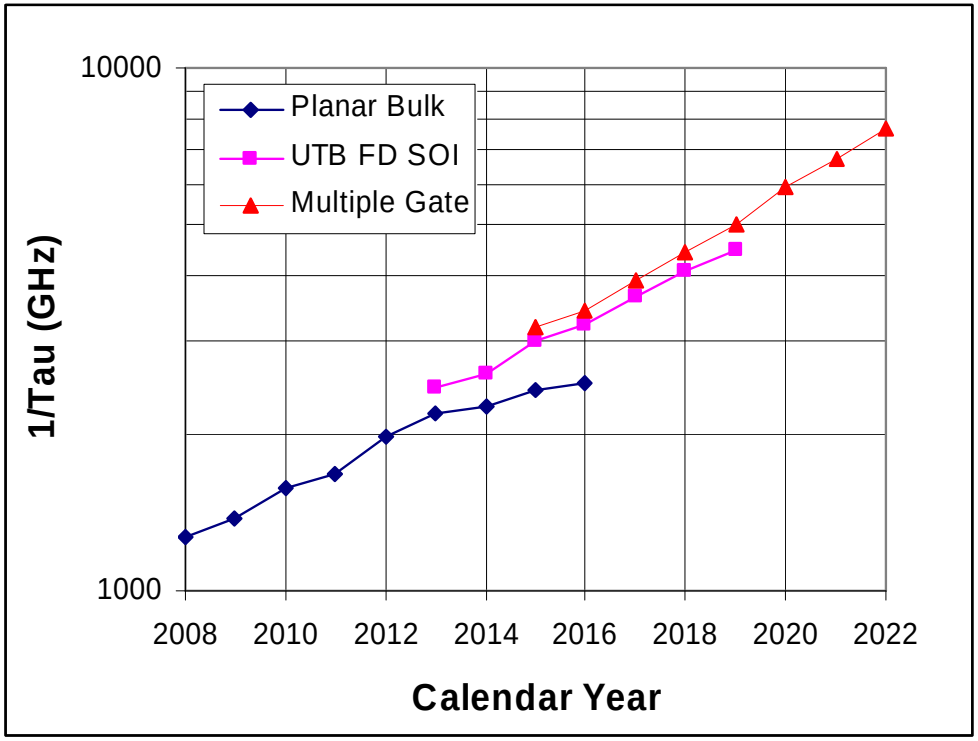
Scaling: The Good, Bad and Ugly

- Good:
  - Higher density
  - Higher performance & throughput
  - More features & functionality
  - Lower power per function
  - Lower cost per function

- Bad and Ugly:
  - Higher development cost development
  - Higher unit cost (wafer)
  - Increasing complexity
  - Increasing variability
  - Higher total power (for fixed die size)

ITRS Performance Scaling

From 2008 ITRS Update



- Introduction of multigate transistor (MuGFET) delayed to 2015
- Lgate scaling slowing to ~0.71x every 3.8 years
- Intrinsic speed increase of ~13% per year, down from ~17% per year

The Ideal Routing Switch

"Ideal" Routing Switch Attributes

Parameter	Value
Non-volatile	Yes
Number of Terminals	2 or 3
On Resistance	< 500 Ohms
Off Resistance	> 1E9 Ohms
Program/Erase Time	>1000 cells/us
Program Current	<100 uA
Program Voltage	> Vcc
Erase Voltage	> Vcc
Operating Temp Range	From -40 C to 125 C
Lifetime	10 years
Placement of switches	No restriction
SEU	no SEU
on/off cycles	>10,000
Availability	Lead process node

- Lower Vcc and higher leakage pose increasing challenges for implementing FPGA routing switch.
- Replacement of routing pass gate could enable significant performance/power benefit.

Process Technology: Friend or Foe?

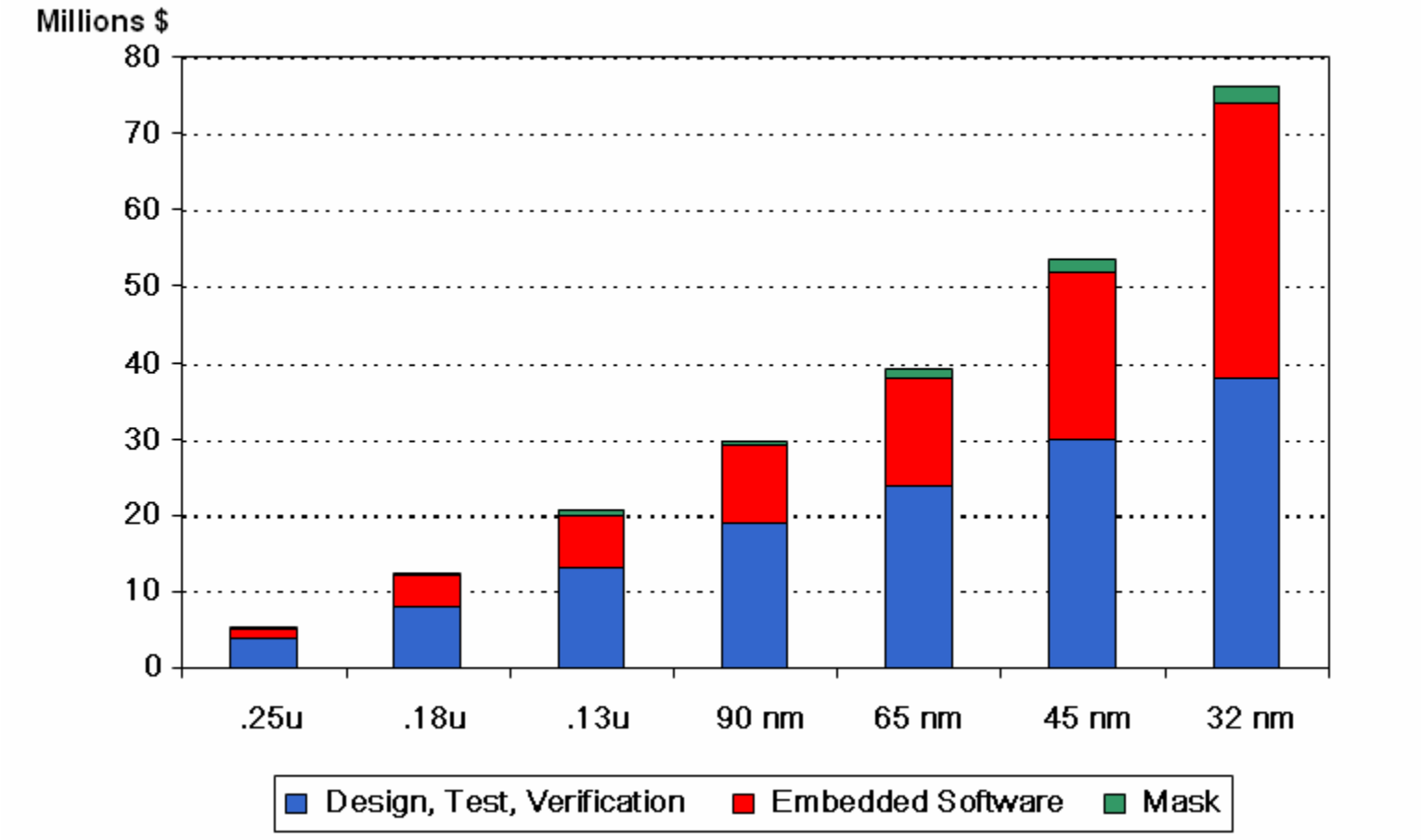
- **Adopting advanced process technologies**

  Increased complexity and slow down in benefits?

- **But ……..**

We have opportunities ahead like never before

Estimated Development Costs Complex ASSP SoC Designs



Gartner

Semiconductor Industry Update October 2008

Chip Development Business Model

- Cost:
  - Development cost: NRE
  - Unit cost: COGS
- FPGA versus ASIC/ASSP:
  - Trade off of NRE and COGS
  - Low volume: emphasis on NRE reduction
  - High Volume: emphasis on COGS reduction
- Reality check – an example:
  - R&D = $100M
  - Market Share = 20%
  - ASP = $20
  - R&D = 20% of revenue
  - ➔ **TAM = $2.5B** (there are not too many markets of this size)
  - **Many low volume ASIC/ASSP providers have a broken business model**
    - **The financial model is not sustainable**
    - **The situation is exasperated with increased R&D cost for newer technologies**

ASIC % Design Starts by Technology

Integration, Lower Cost, Performance ↑

Process Node	2002 %	2003 %	2004 %	2005 %	2006 %	2007 %	2008 %	2009 %	2010 %	2011 %	Dev. Costs $M
0.022 µm	0	0	0	0	0	0	0	0	0	0	110
0.032 µm	0	0	0	0	0	0	0	1	2	2	80
0.040 µm	0	0	0	0	0	1	2	4	6	7	60
0.045 µm	0	0	0	0	0	1	2	4	6	7	60
0.065 µm	0	0	0	1	2	6	8	10	13	15	55
0.09 µm	0	1	8	13	18	23	23	24	24	24	30
0.13 µm	18	37	42	29	29	27	27	25	24	24	20
0.18 µm	38	27	23	20	17	14	12	10	10	8	13
0.25 µm	16	15	12	12	11	9	9	8	7	6	5
0.35 µm	21	16	12	12	11	10	8	8	6	5	3
0.5 µm	5	4	3	7	7	6	6	5	4	4	2
L>0.5 µm	1	1	0	6	6	6	5	5	5	5	<1
Total	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	

Increased Risks & Development Cost ↑

#1 ASIC Design Technology

Source: Altera & Gartner

ASIC % Design Starts by Technology

Integration, Lower Cost, Performance ↑

Process Node	2002 %	2003 %	2004 %	2005 %	2006 %	2007 %	2008 %	2009 %	2010 %	2011 %	Dev. Costs $M
0.022 µm	0	0	0	0	0	0	0	0	0	0	110
0.032 µm	0	0	0	0	0	0	0	1	FPGA	FPGA	80
0.040 µm	0	0	0	0	0	1	FPGA	FPGA	6	7	60
0.045 µm	0	0	0	0	0	1	2	4	6	7	60
0.065 µm	0	0	0	1	2	FPGA	8	10	13	15	55
0.09 µm	0	1	8	FPGA	FPGA	23	23	24	24	24	30
0.13 µm	FPGA	FPGA	FPGA	29	29	27	27	25	24	24	20
0.18 µm	38	27	23	20	17	14	12	10	10	8	13
0.25 µm	16	15	12	12	11	9	9	8	7	6	5
0.35 µm	21	16	12	12	11	10	8	8	6	5	3
0.5 µm	5	4	3	7	7	6	6	5	4	4	2
L>0.5 µm	1	1	0	6	6	6	5	5	5	5	<1
Total	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	

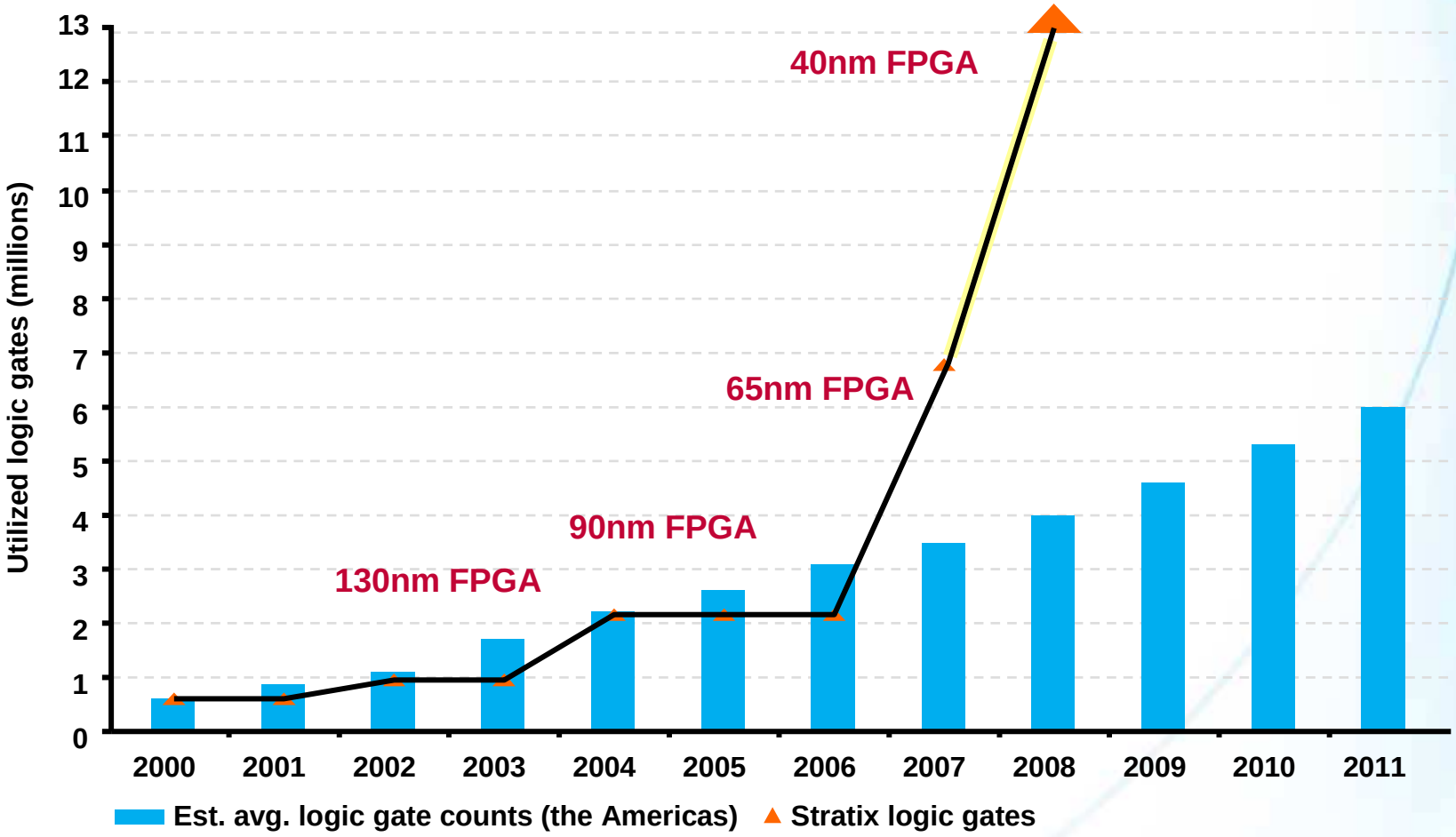
Increased Risks & Development Cost ↑

#1 ASIC Design Technology

#1 PLD Design Technology FPGA

Source: Altera & Gartner

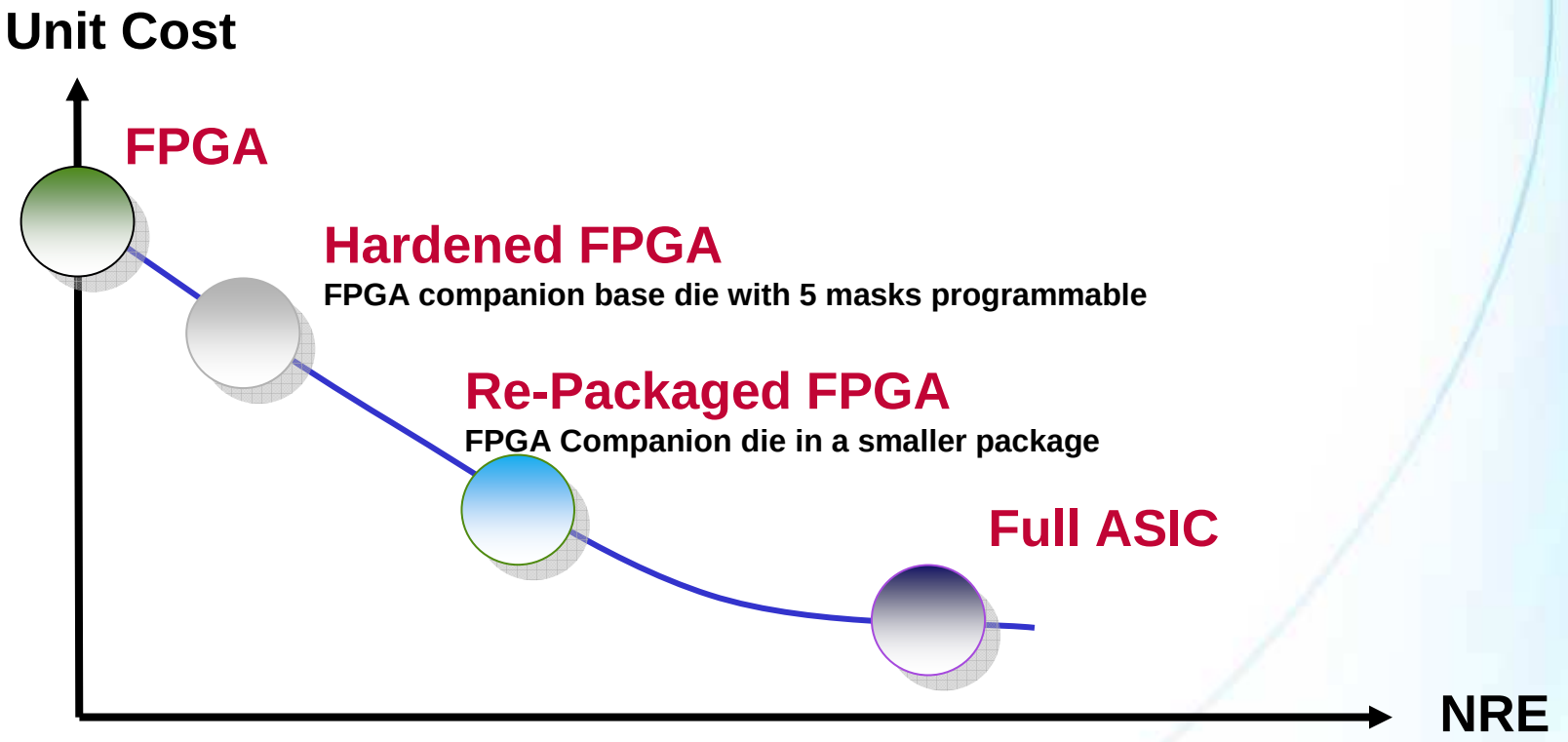
Average ASIC Density



Note: Data based on Gartner Dataquest

FPGA to Full ASIC Path

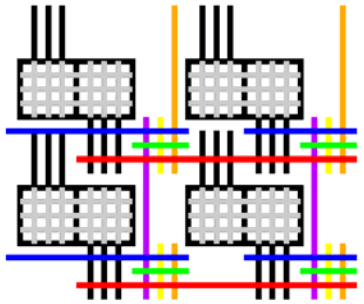
- Solution points in NRE – Unit Cost Space
  - Rationalized volume forecast is the key to strategy



Summary

- Significant challenges exist for technology scaling
  - We are in the era of power-constrained scaling
  - Variability will continue to increase
- Innovations expected to enable continued scaling
  - HKMG, MuGFETs, high-mobility channels, …
- But they increase complexity and cost
- Bifurcation in ASIC/ASSP offerings
  - Only a small portion can afford adopting advanced technologies

- **This is all music for FPGA**
  - The most significant opportunities for FPGA is in share gain from ASIC & ASSP
  - Advanced process technologies are tipping the scale in favor of FPGA
  - **We are at an inflection point**



CMOS vs. Nano
FPGA2009 Panel

André DeHon

andre@seas.upenn.edu

Penn

Position

1. Beneficial to work with nature (physics).
2. Atomic-scale is noisy and statistical.
3. Fine-grained reconfiguration and continuous adaptation are powerful.
4. Regularity is good.
5. Randomness can be harnessed for good.
6. Lithographic CMOS is the new PCB.

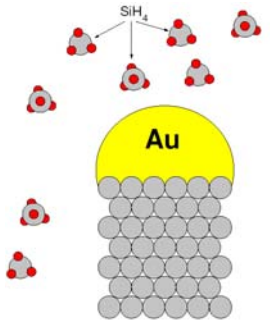
Beneficial to work with nature

- …rather than against it.
- Atomic-scale offer:
  - New switching/communication phenomena
  - New ways to define structures, dimensions, and spacing
  - New ways to perform assembly

Beneficial to work with nature

See: http://www.dna.caltech.edu/Papers/DNAorigami-nature.pdf
for some wonderful images of DNA Assembly and details on how to perform the assembly.

See: http://physci.llnl.gov/Research/qsg-090205/carbonNanotubes.html
for images of CNT growth.



- Deeper understanding atomic-scale physics
  - Increases our palette → better solutions
    - Favorable E,D,A tradeoffs, cheaper manufacture

Beneficial to work with nature

- …but today, we are stumbling our through it like clumsy, ignorant giants

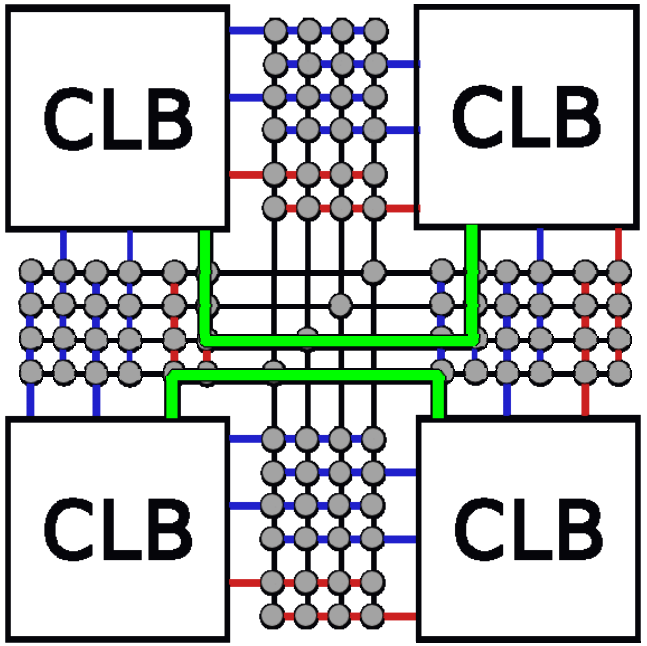
Atomic-scale is noisy and statistical.

- The **nature** of atomic-scale elements is statistical.
  - ➔ anything we build a this scale
    - Lithographic or bottom up
  - ….will behave statistically
    - kT, uncertainty principle, tunneling, ….
- Will lead to
  - Defects, Variation, Misbehavior
- Current approaches are brute force attempts to hide this nature
  - Millions of electrons, thousands of dopants, large noise margins.

…work with nature
not against it.

Fine-Grained Reconfiguration

- Selecting devices→role mapping **after** fabrication is powerful.
  - Mitigation fabrication statistics
    - Defects
    - variation
  - Mitigate lifetime changes



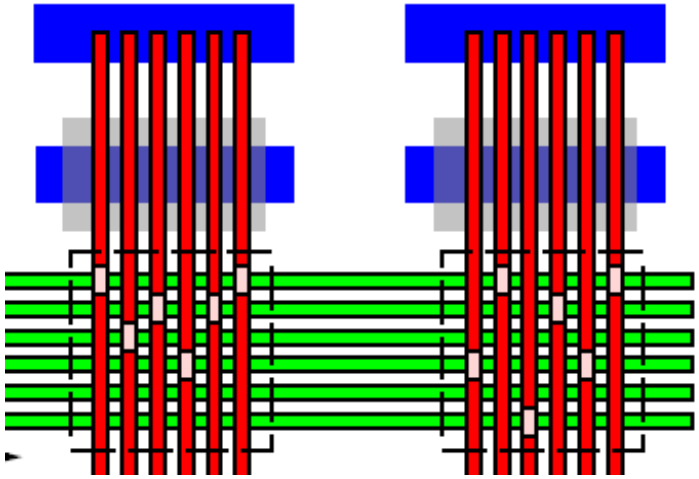
- **FPGA-like** architectures have a potential head-start over alternatives.

Regularity

- Regular structures easier to self-assemble
  - Low information content
  - Exploit natural phenomena
- E.g.
  - **Large area 50 nm period grating by multiple nanoimprint lithography and spatial frequency doubling.** B Cui, Z Yu, H Ge, and SY Chou, *APPLIED PHYSICS LETTERS*, **90**, 043118 (2007)
  - http://www.research.ibm.com/journal/rd/515/black.html
  - Large-Scale Hierarchical Organization of Nanowire Arrays for Integrated Nanosystems. D. Whang and S. Jin and Y. Wu and C. M. Lieber, Nanoletters, 3(9):1255—1259, Sept. 2003.

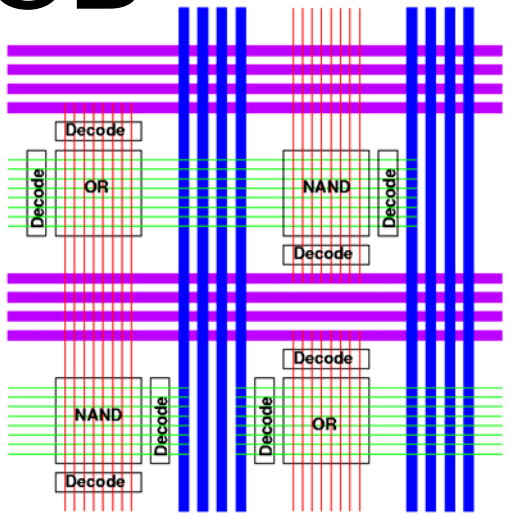
- **FPGA**-like architectures exploit regularity
  - While providing diversity for computation

Randomness

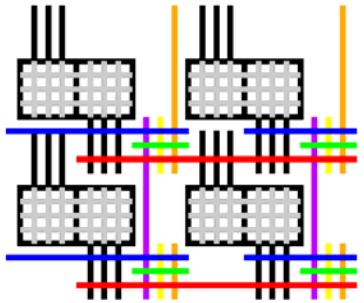


- Can be a tool for good
  - Diversity creation
  - Expanders (LDPCs, network routing)
  - CAD
  - Randomized Algorithms
  - Heavily exploited by nature
    - …work with nature.

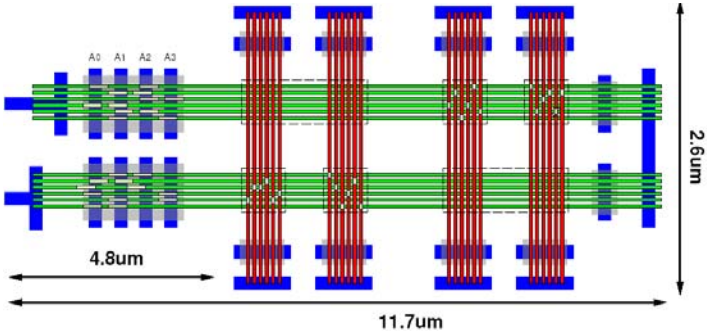
CMOS is the new PCB



- Differential Reliability
  - Islands of stability & determinism
    - diagnose, supervise, configure
- Lithographic CMOS does this well
- Provides the substrate on which atomic-scale things can be assembled
- **Goal:** reliability of CMOS with {E,D,A} of atomic-scale building blocks
  - Compare DRAM memories



Position



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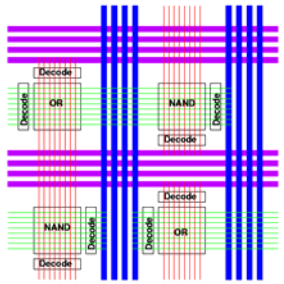


Nano-electronics for Near-Future FPGA

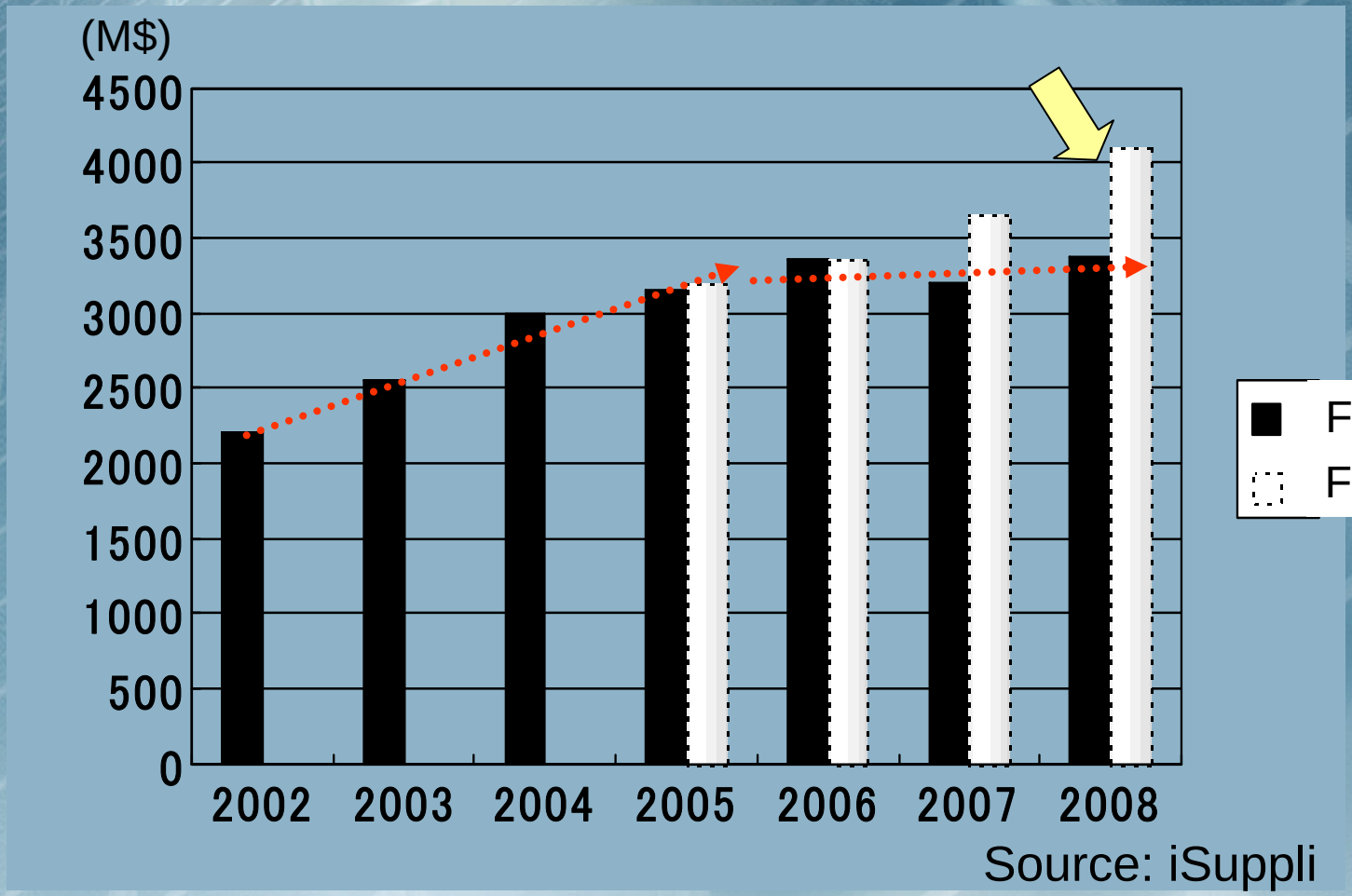
Shinobu Fujita

Corporate R&D Center
Toshiba Corporation

R&D of Nano-electronics and their Applications

TOSHIBA
Leading Innovation

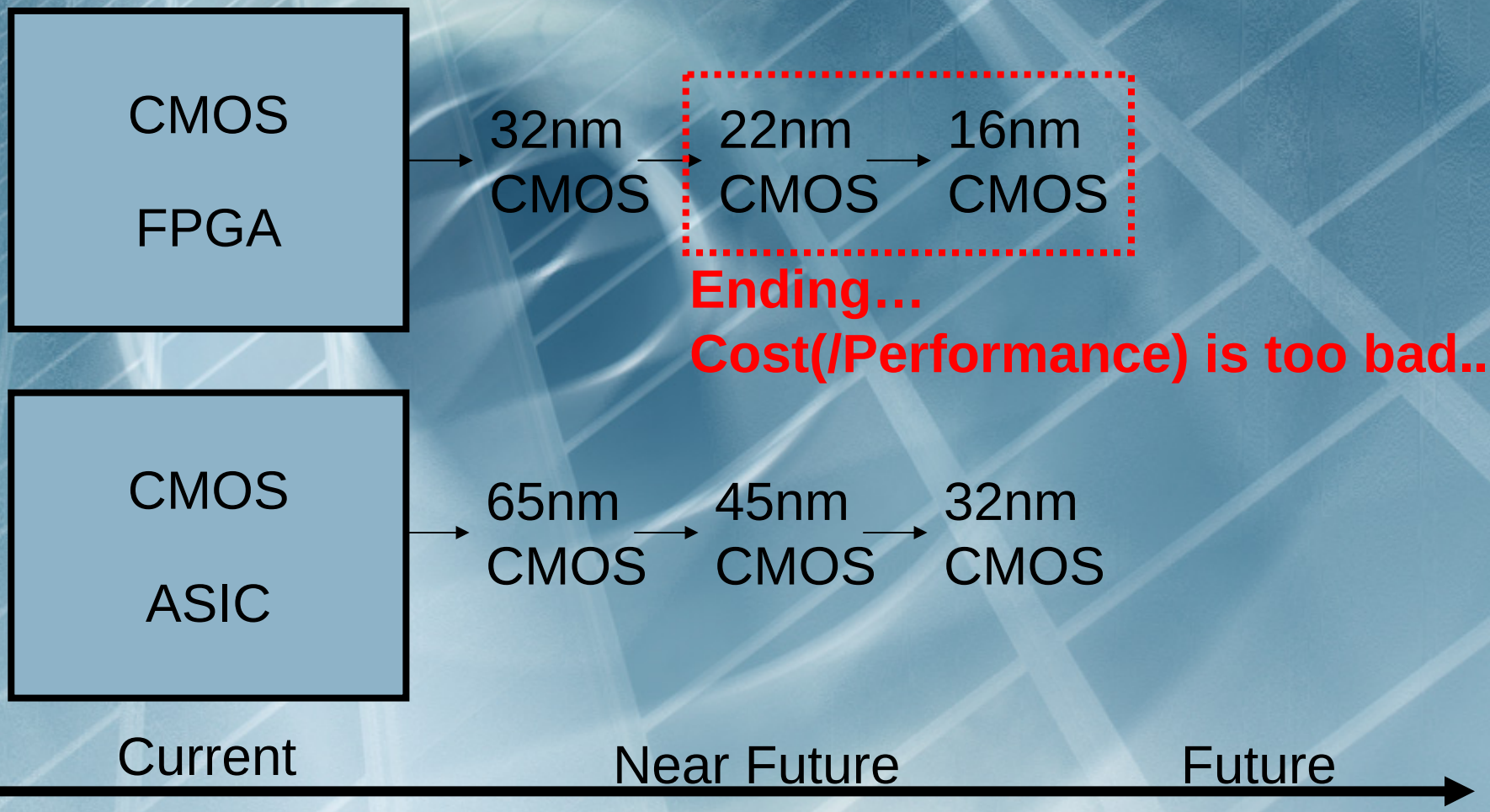
FPGA needs something other than CMOS scaling for future?



Source: iSuppli

FPGA cannot replace ASIC enough..
(Power, Area, Speed..)

FPGA vs ASIC after CMOS ending



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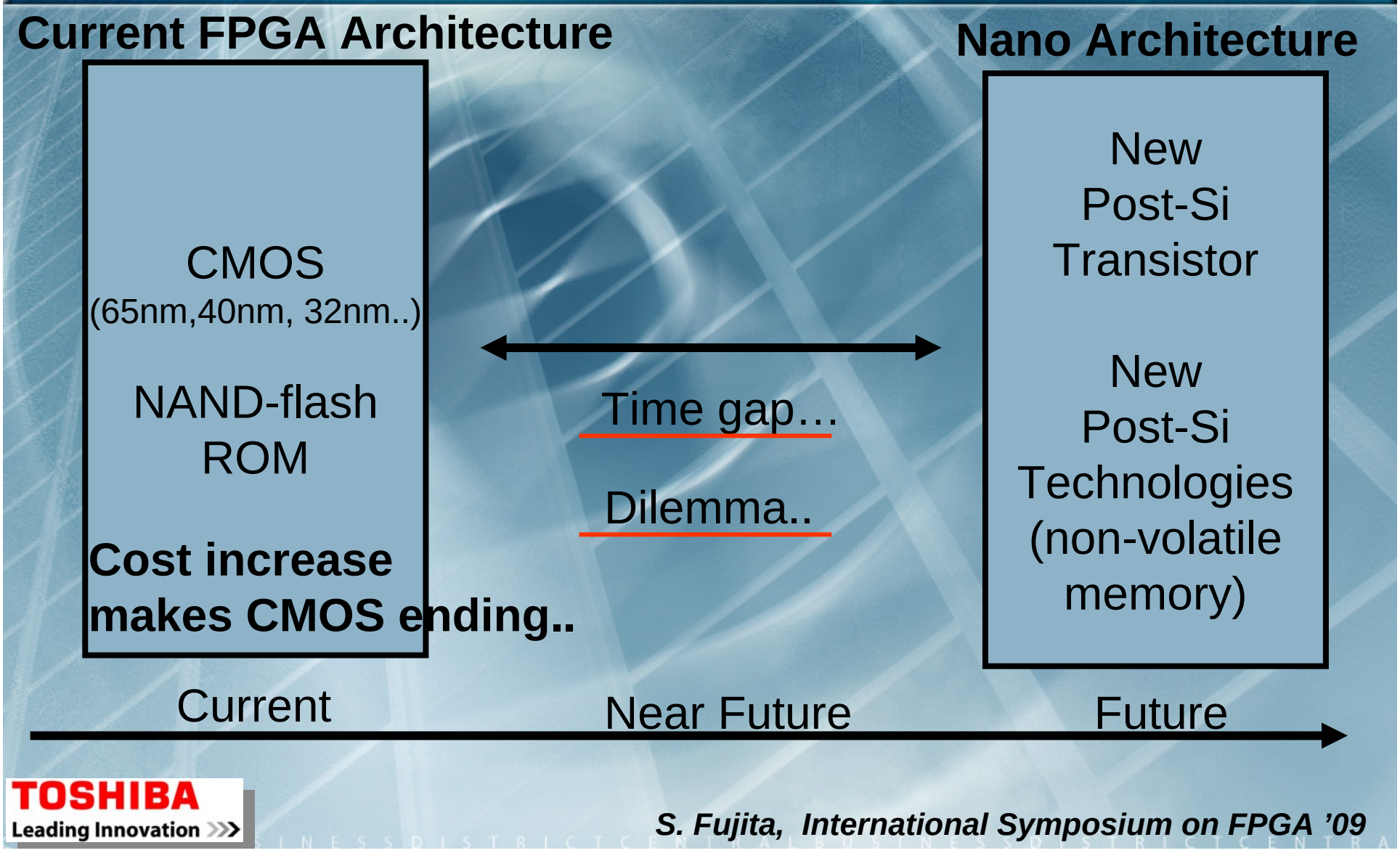
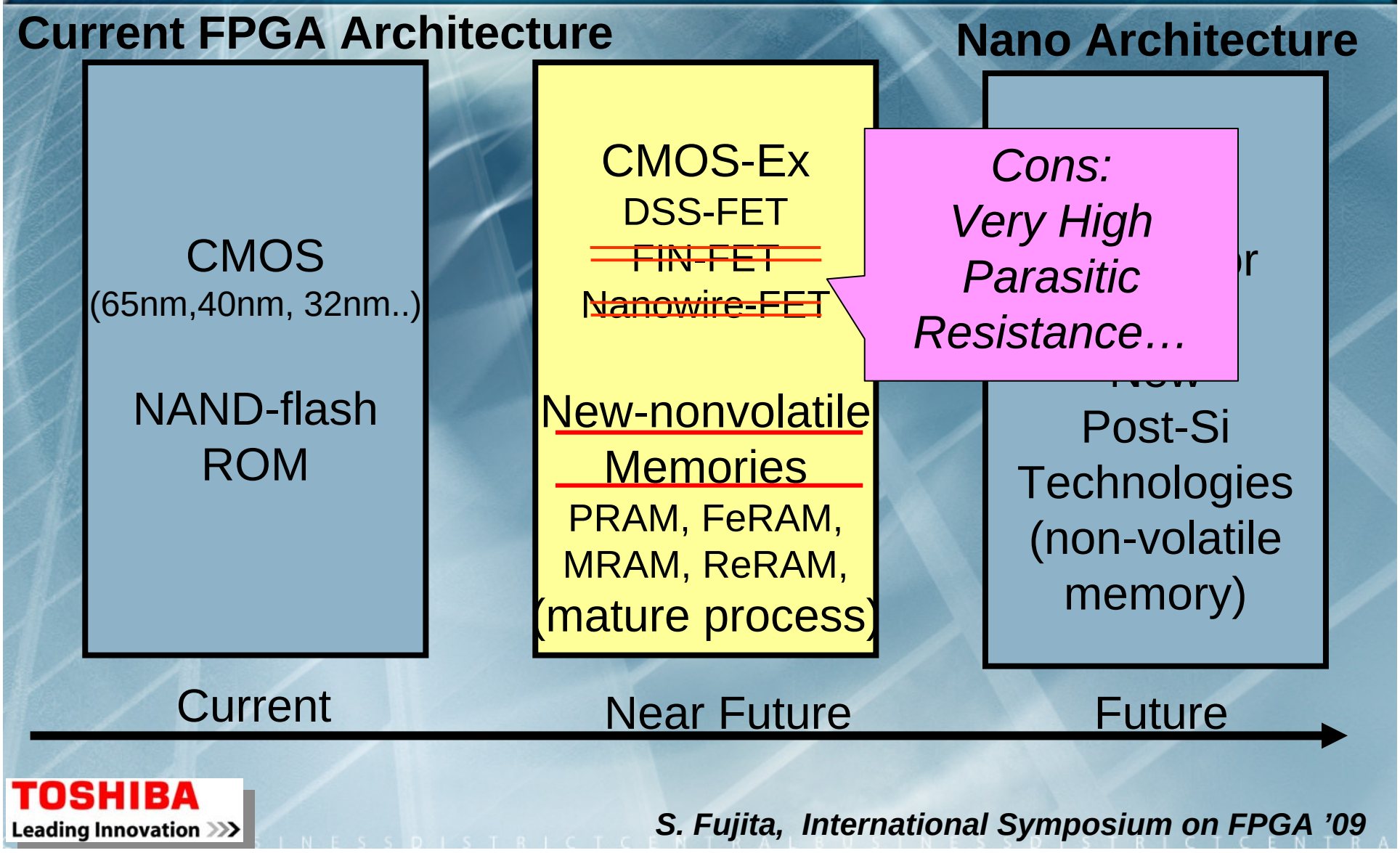
Leading Innovation

S. Fujita, International Symposium on FPGA '09

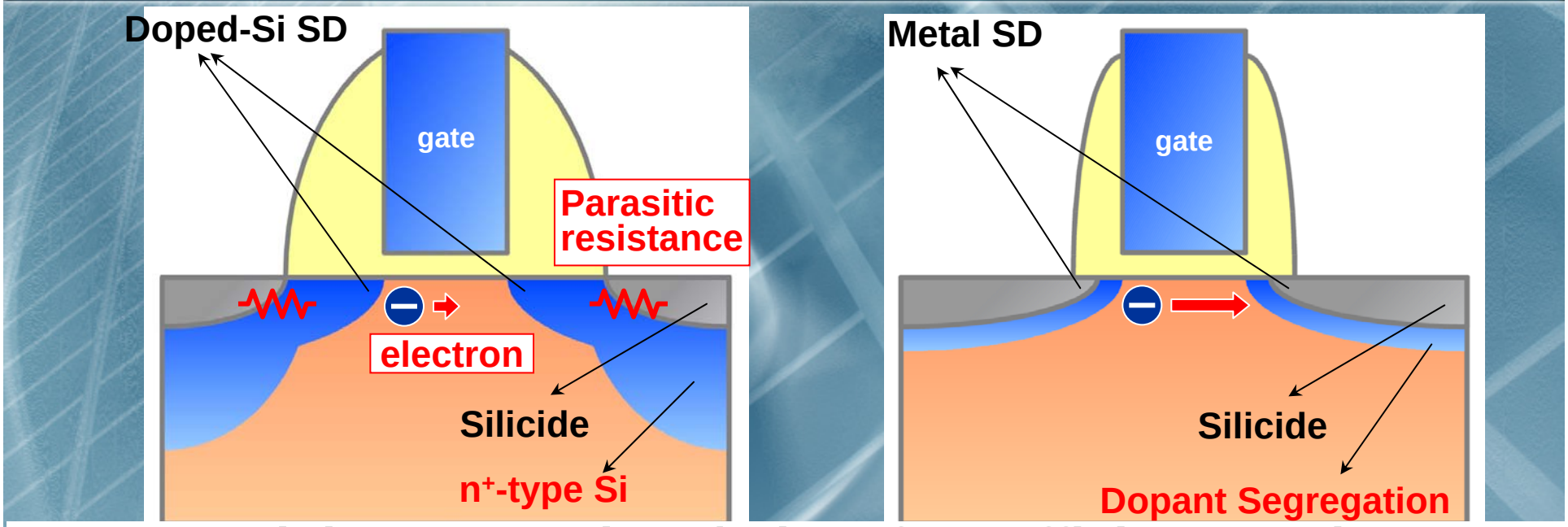
Gap between current FPGA and Future Nano-electronics?



Solutions for Near Future FPGA!



CMOS-Ex for FPGA
Dopant Segregated Schottky (DSS) MOSFETs



Segregated dopants at the S/D interface efficiently reduce Schottky barrier height.

Low Source/Drain resistance

(Superior performance of PASS Transistor logic!!)

- **Short channel effect immunity**
- **Enhanced carrier injection velocity**

(A. Kinoshita et al, (Toshiba), IEDM 2006)

CMOS-Ex for FPGA
Dopant Segregated Schottky (DSS) MOSFETs

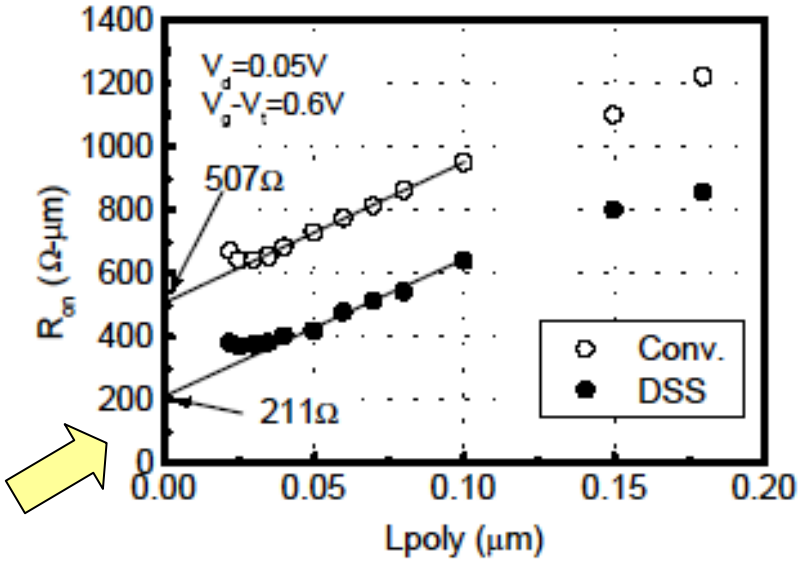
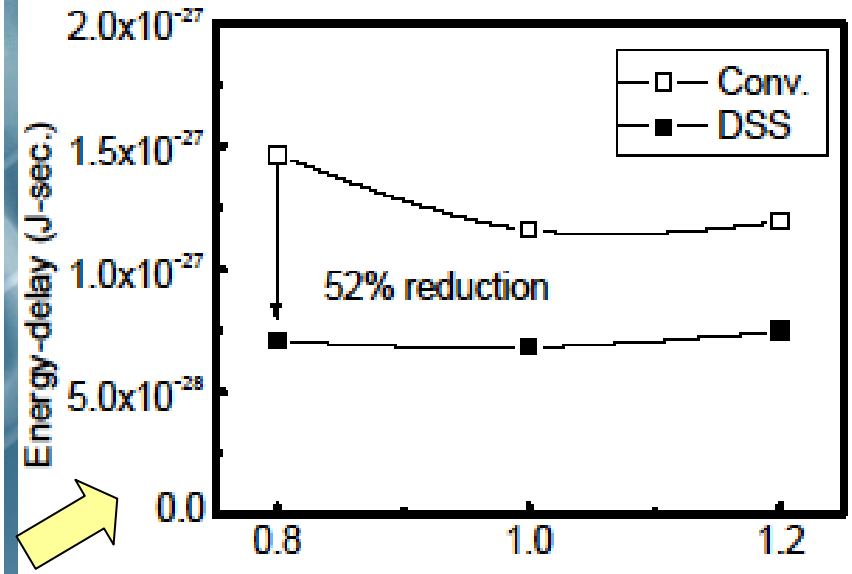


Fig. 7. Rtotal - Lpoly plots in the linear region for DSS and conv. FET



(a) 3-input NAND

Superior performance of PASS Transistor logic!!
Also, CMOS performance is superior to conventional one.

(T. Kinoshita et al, (Toshiba), IEDM 2006)

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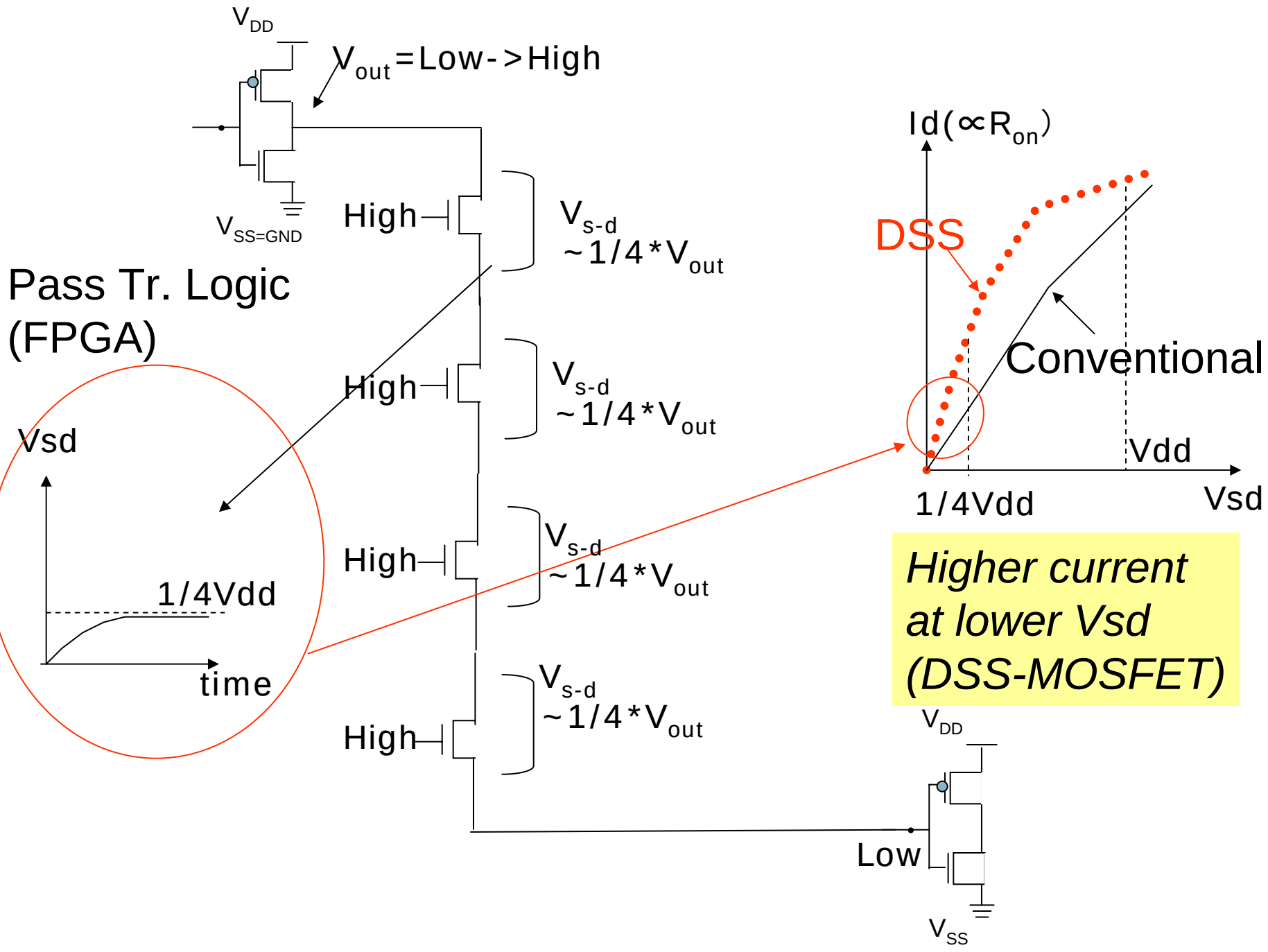
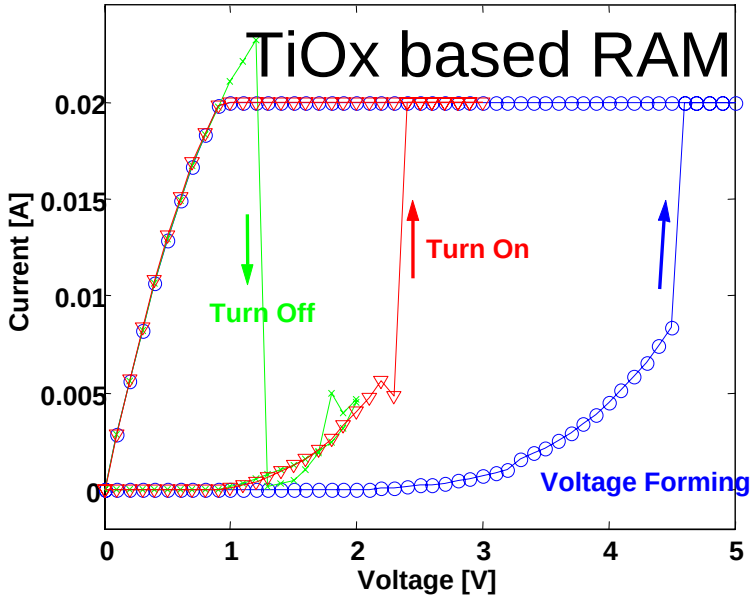
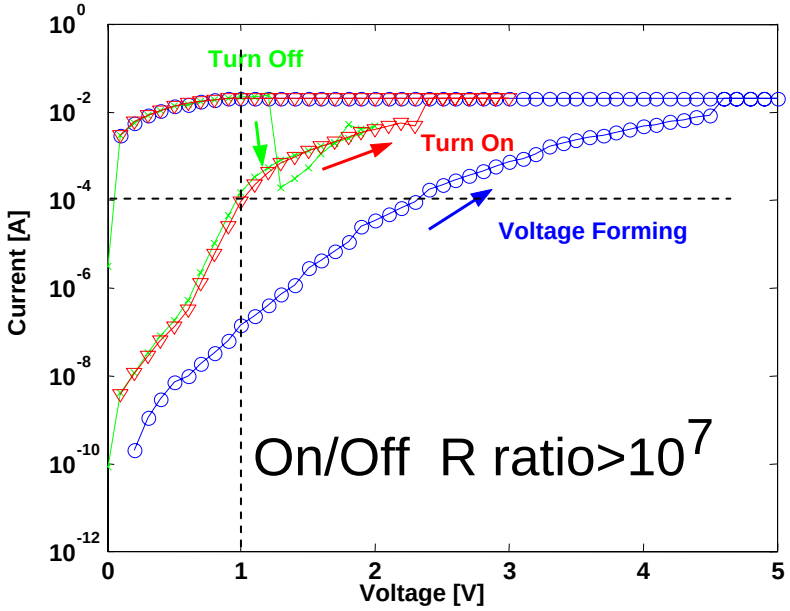
Leading Innovation

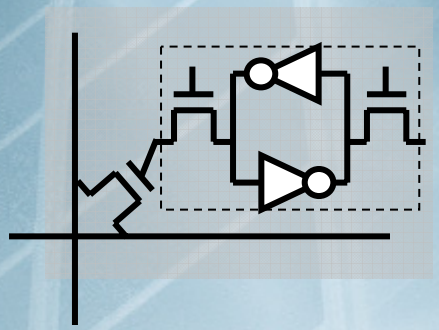

V_{DD}
V_{out}=Low->High
$V_{SS=GND}$
Pass Tr. Logic
(FPGA)
High
High
High
High
V_{s-d}
~1/4*V_{out}
V_{s-d}
~1/4*V_{out}
V_{s-d}
~1/4*V_{out}
V_{s-d}
~1/4*V_{out}
Vsd
1/4Vdd
time
Id(∝R_{on})
DSS
Conventional
Vdd
1/4Vdd
Vsd
Higher current at lower Vsd (DSS-MOSFET)
V_{DD}
Low
V_{SS}

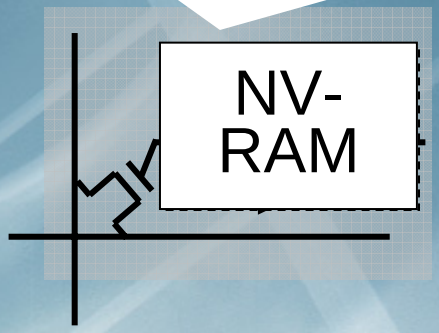
New-nonvolatile Memories for FPGA

W. Wong et al,(Stanford, Toshiba) IEDM 2006









Reduce Power & Area

SRAM-based configuration

Non-Volatile-RAM-based

TOSHIBA
Leading Innovation

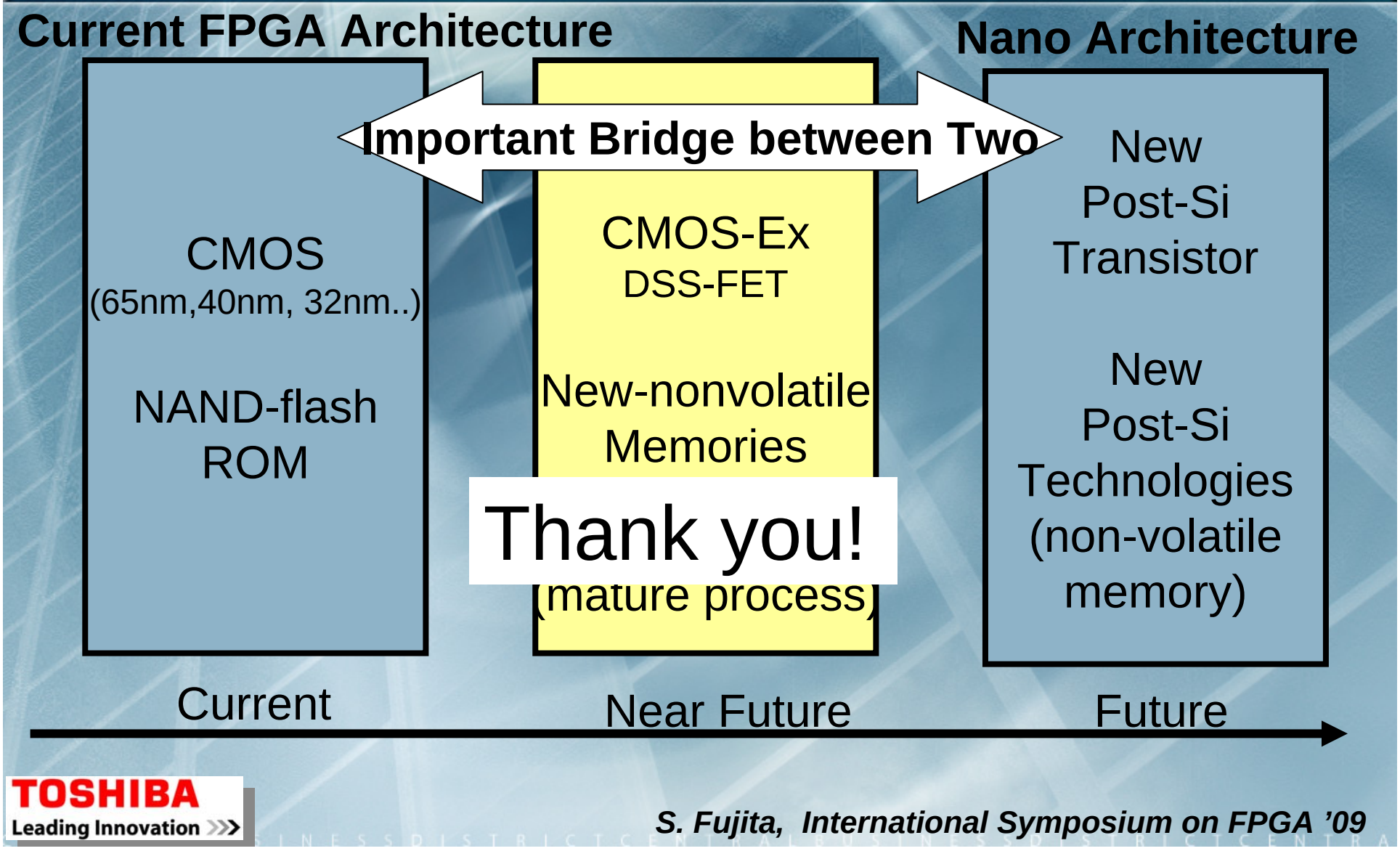
S. Fujita, International Symposium on FPGA '09

Requirement to NV-RAM for replacing config-SRAM

- High off-Resistance (to reduce leakage current)
  (<100pA, = 1V/10Gohm!) @100x100nm2
- High On/Off ratio …. At least >100, or $>10^6$
- Programming voltage: higher than Vdd of CMOS
- Long-term retention: > 10years
- Long-term reliability: NO memory disturbance during logic operation
- Plus.. decreasing programming current

Different requirements from those for memory circuits!

Conclusion
Solutions for Near Future FPGA!



FPGA '09 Evening Panel
CMOS vs. Nano: Comrades or Rivals?

CMOS Extension and "Beyond CMOS" Information Processing Technologies

February 23, 2009

Jim Hutchby - SRC

FPGA '09 Evening Panel
CMOS vs. Nano: *Neither* -They are Family

CMOS Extension and "Beyond CMOS" Information Processing Technologies

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FPGA '09 Evening Panel
CMOS IS NANO

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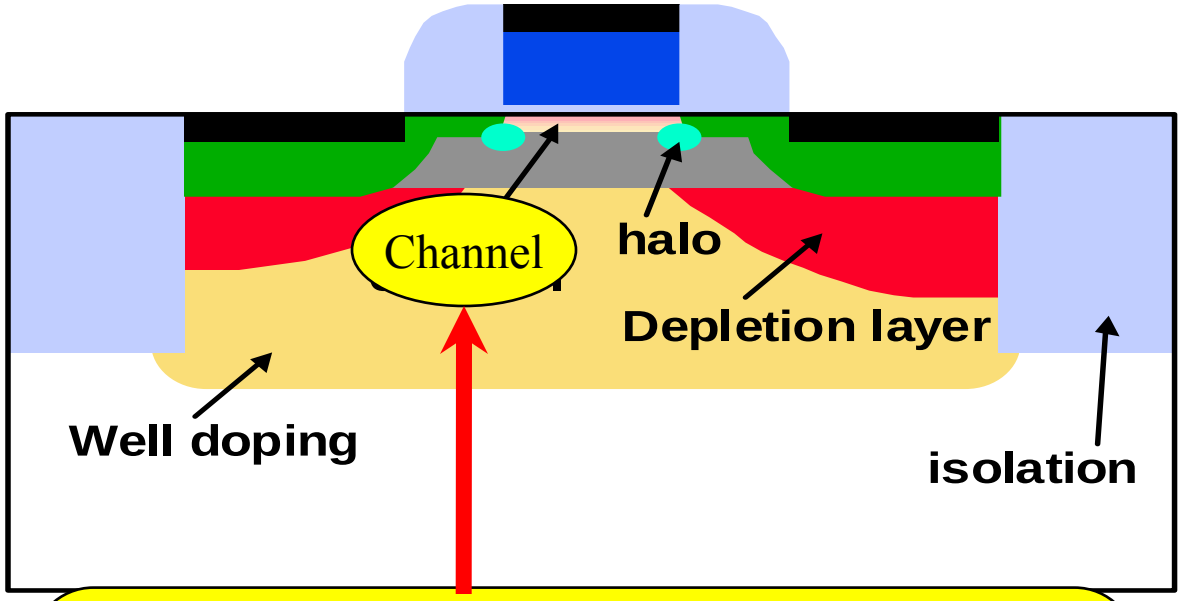


- Critical dimension < 100nm
  - Gate length & Channel thickness
- New physics for nano device
  - Quantum confinement in channel

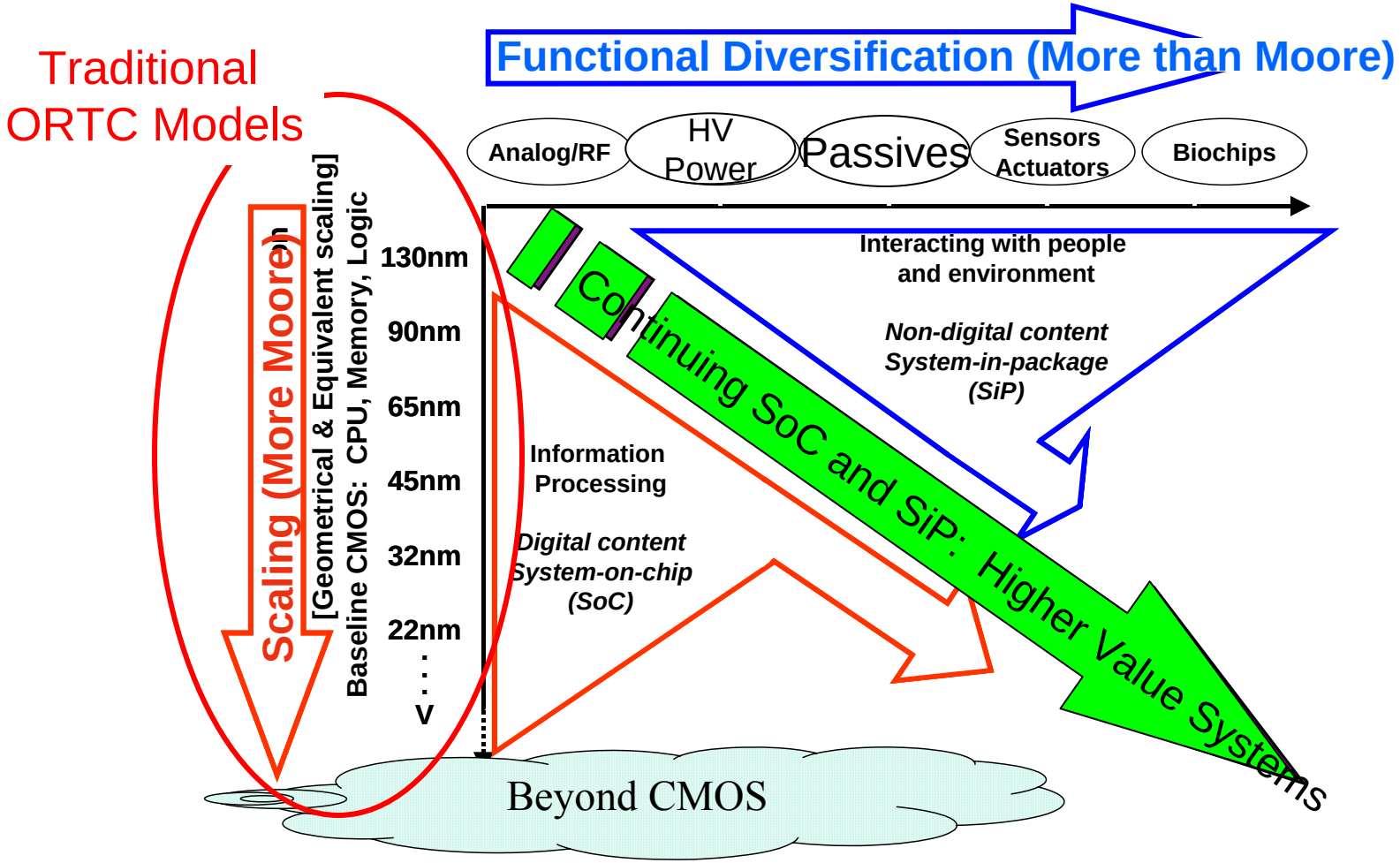
End of the Road map??

The Reign of CMOS Continues – Geometrical Scaling will Shift to Functional Scaling

- ITRS ERD & ERM are evaluating devices and technologies to extend CMOS to and beyond 2024
- ITRS ERD & ERM are looking for novel solutions for information processing for applications beyond 2024
  - Integrated with CMOS platform
  - Eventually stand alone
- Heterogeneous integration of diverse functions (e.g., NEMS, Sensors, Analog, RF, Bioelectronics, etc.) in "Functional Diversification" is changing technology requirements for integrated electronics..

2007 ITRS Executive Summary

Moore's Law & More



Content Source: ITRS 2008 Update Public Conference Draft 0 – December, Seoul Korea

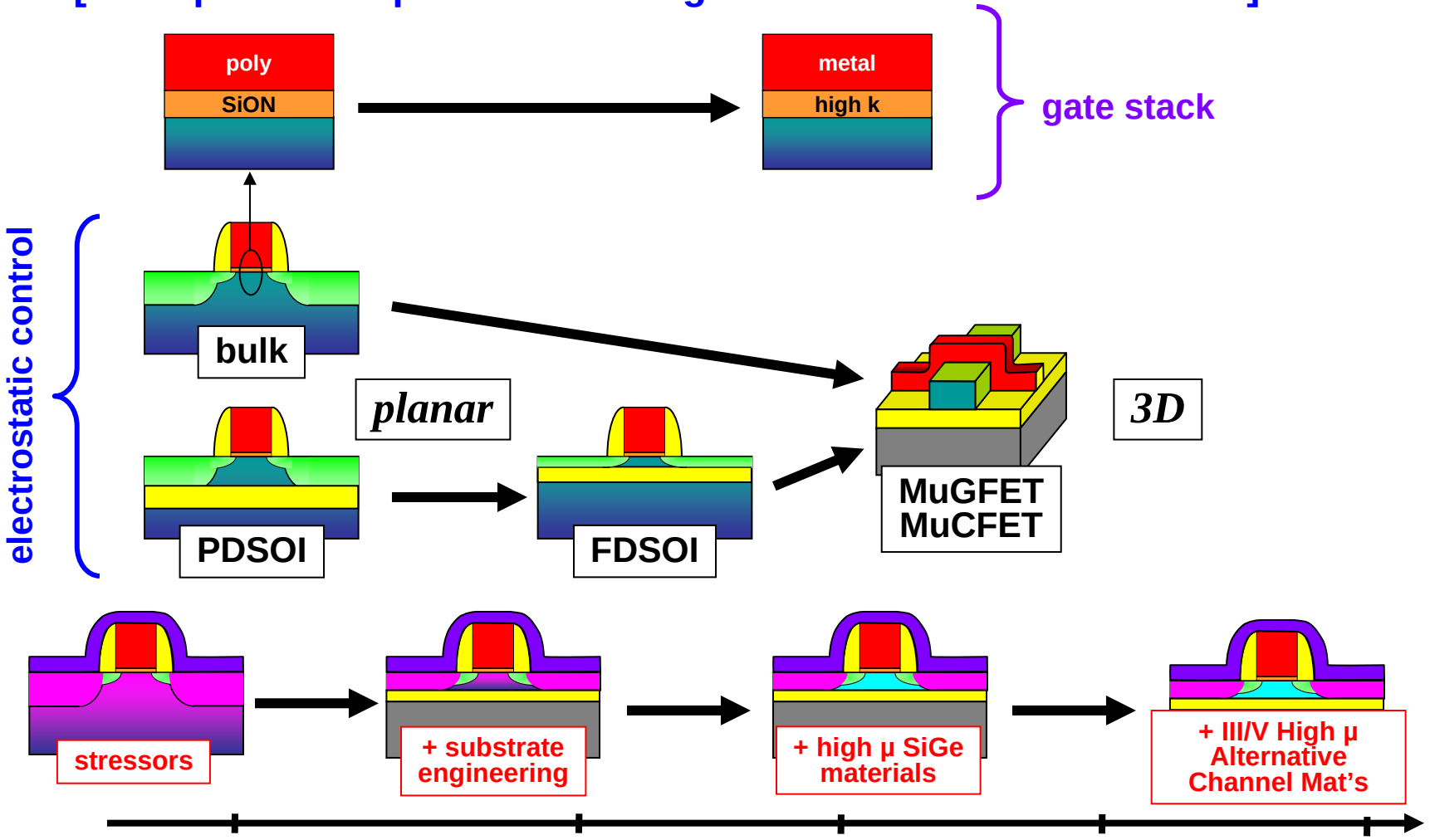
2007 High Performance Logic Roadmap
Illustrating Need for New High-velocity Channel Materials

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*		
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*		
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*	*9*	*8*	*7*	*6*	*6*		
Lg: Physical Lgate for High Performance logic (nm) [1]	**25**	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**	**9**	**8**	**7**	**6**	**5.5**	**5**	**4.5**
Effective Ballistic Enhancement Factor , Kbal [12]																
Extended Planar Bulk	**1**	**1**	**1**	**1**	**1**	**1**										
UTB FD				**1.05**	**1.1**	**1.16**	**1.2**	**1.24**	**1.28**							
DG					**1.17**	**1.25**	**1.31**	**1.37**	**1.53**	**1.67**	**1.87**	**1.99**	**1.97**	**2.11**	**2.11**	**2.11**

Ultimate CMOS scaling needs new channel materials with enhanced ballistic velocity

2007/08 - PIDS/FEP - Simplified Transistor Roadmap

[Examples of "Equivalent Scaling" from ITRS PIDS/FEP TWGs]



[ITRS DRAM/MPU Half-Pitch Timing:	**65nm** 2007[7.5]	**45nm** 2010	**32nm** 2013	**22nm** 2016	**16nm** 2019]

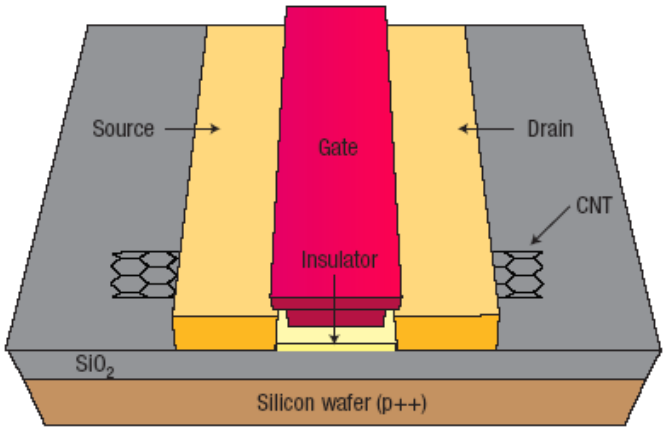
Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

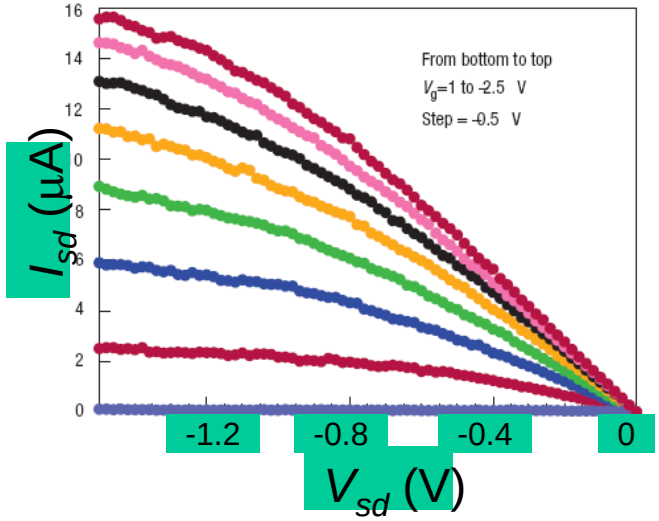
Alternate Channel Materials and Structures for Extending CMOS

Alternate channel materials and structures for extending CMOS beyond silicon & III-V compound semiconductors include:

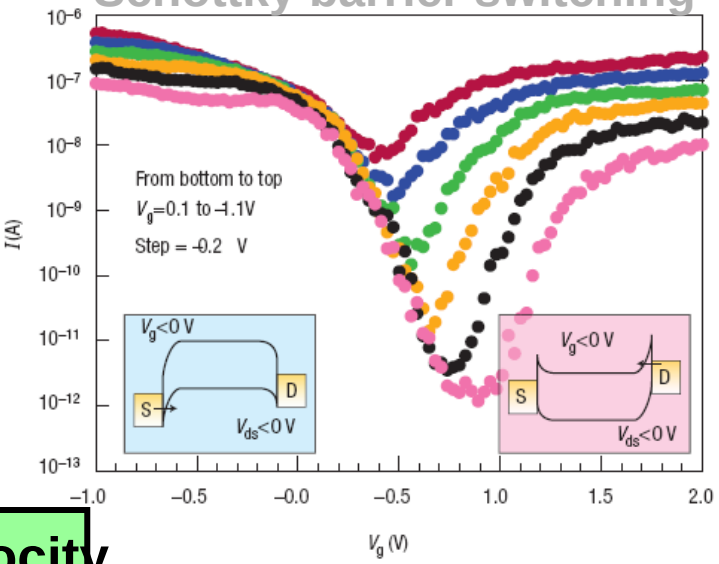
- Nanowires,
- Nanotubes, and
- Graphene

Nanotube FET





Schottky barrier switching

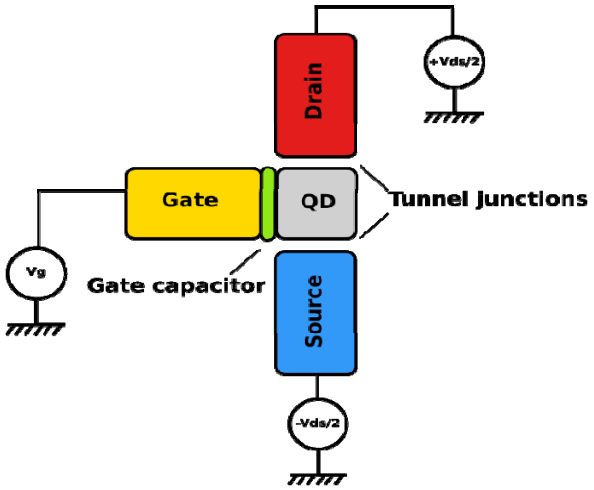


Band gap:	0.5 – 1 eV
On-off ratio:	~ 10^6
Mobility:	~ 100,000 cm^2/Vsec @RT
Ballistic @RT	~ 300-500 nm
Fermi velocity:	10^6 m/sec (V_F)
Max current density	> 10^9 A/cm^2

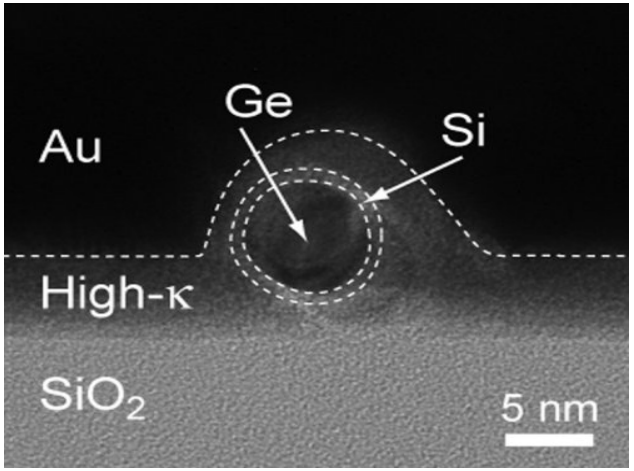
Very High velocity

Ph. Avouris et al, Nature Nanotechnology **2**, 605 (2007)

Nanowire & Single Electron Transistors



Single Electron Transistor



Nanowire Transistor

	Nanowire FET	SET
Channel	1-dimensional	Island/quantum dot
Channel length	5 – 10nm	1 – 10nm[1]
Capacitance	aF	aF
Conductance	Channel resistance or electron-injection limited 10 – 100mS	Tunnel-limited 0.02 – 2mS
Gain	High/marginal	Low[2]
ON/OFF state	Single	Multiple

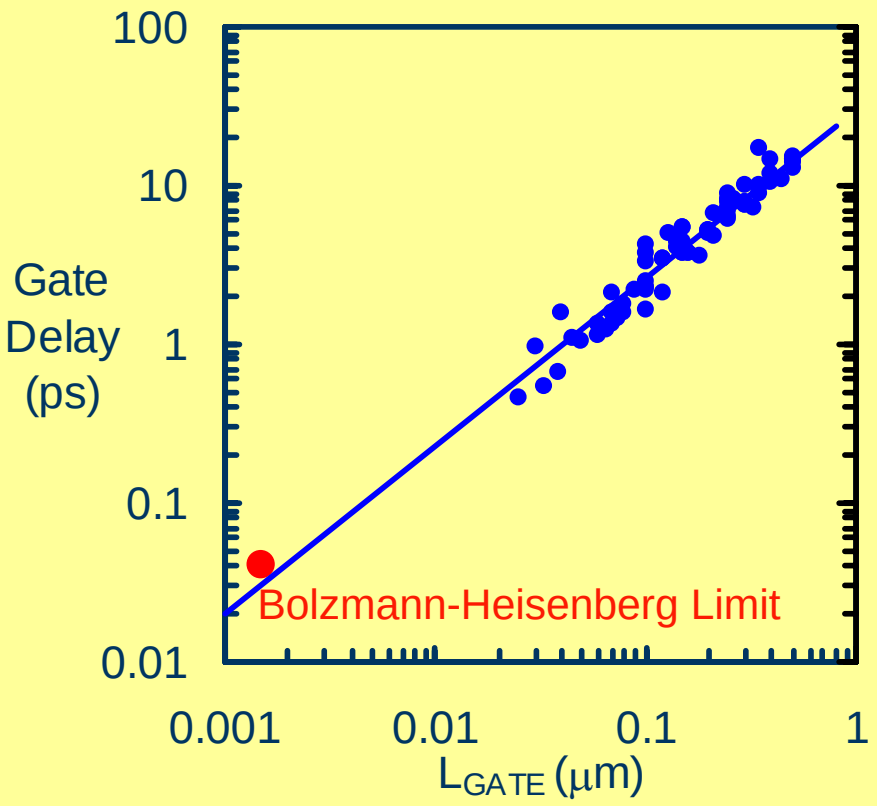
How low can we go?

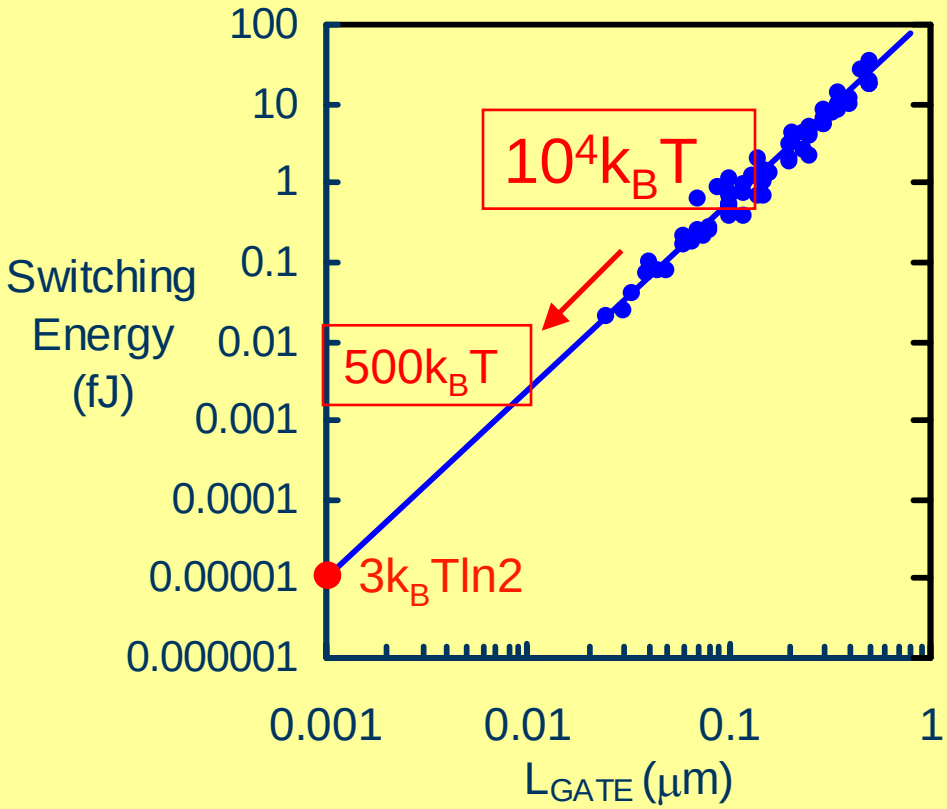
- Future devices could theoretically scale down to
  - 1.5 nm
  - with 0.04 ps switching speeds
  - and 0.017 electron volts in terms of power consumption.

J. Hutchby, G. Bourianoff, et al., *Proc. of IEEE*, 2003

CMOS scaling on track to obtain physical limits for electron devices

George Bourianoff / Intel

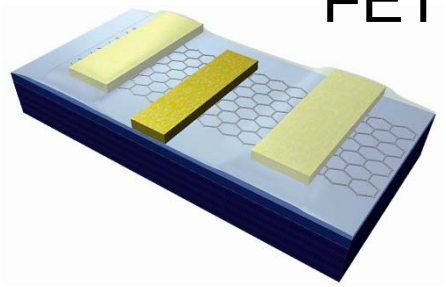




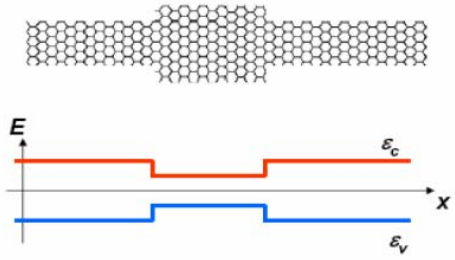
Graphene Electronics: Conventional & Non-conventional

Conventional Devices

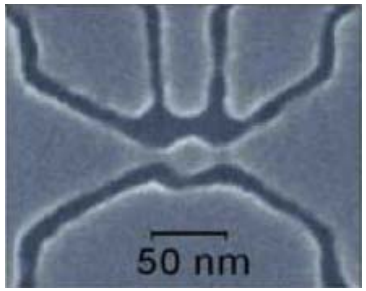
FET



Band gap engineered
Graphene nanoribbons

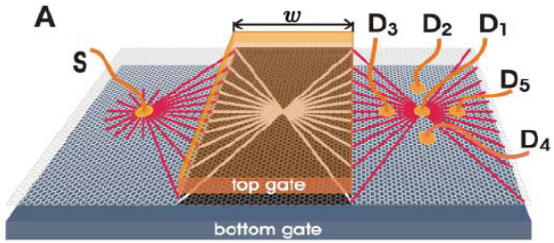


Graphene quantum dot



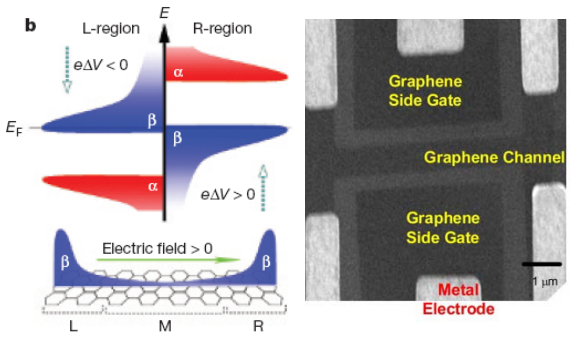
(Manchester group)

Nonconventional Devices



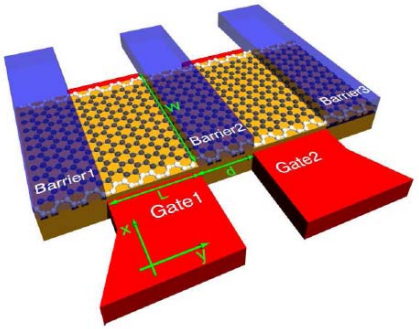
Graphene Veselago lense

Cheianov *et al. Science* (07)



Graphene Spintronics

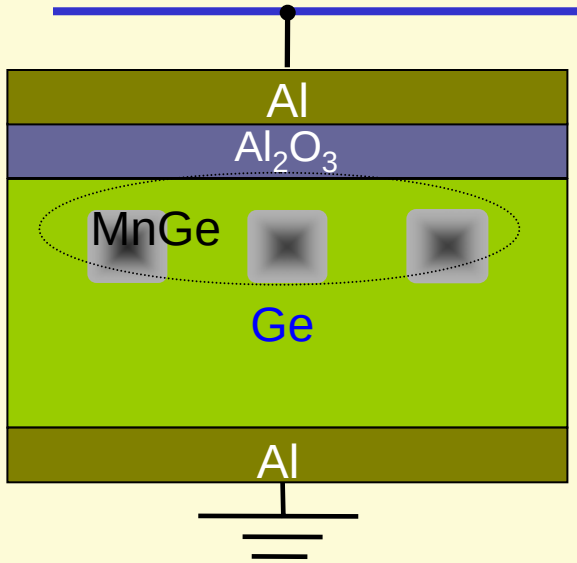
Son *et al. Nature* (07)



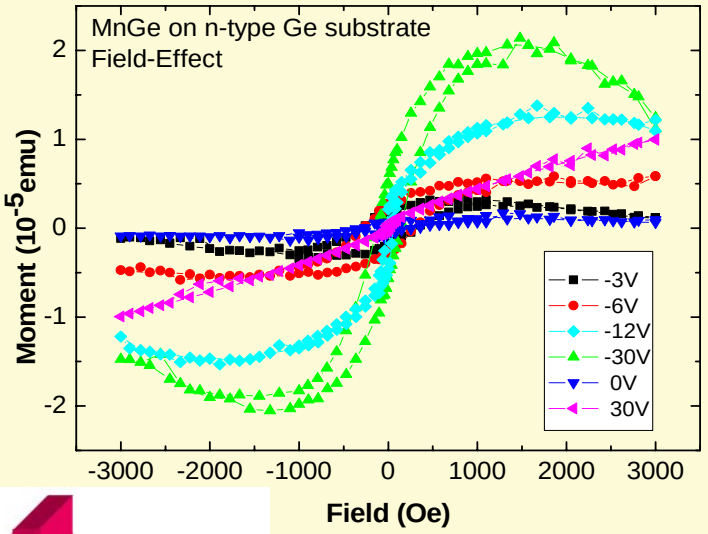
Graphene pseudospintronics

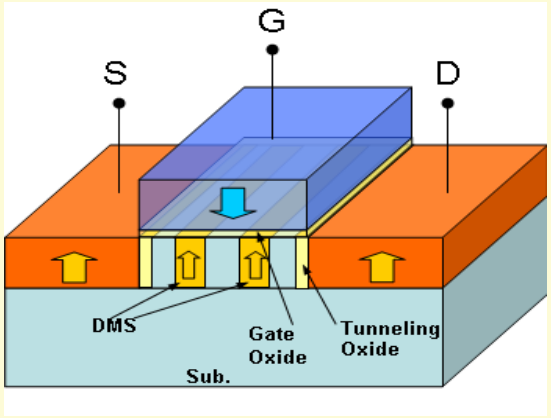
Trauzettel *et al. Nature Phys.* (07)

Spin FET

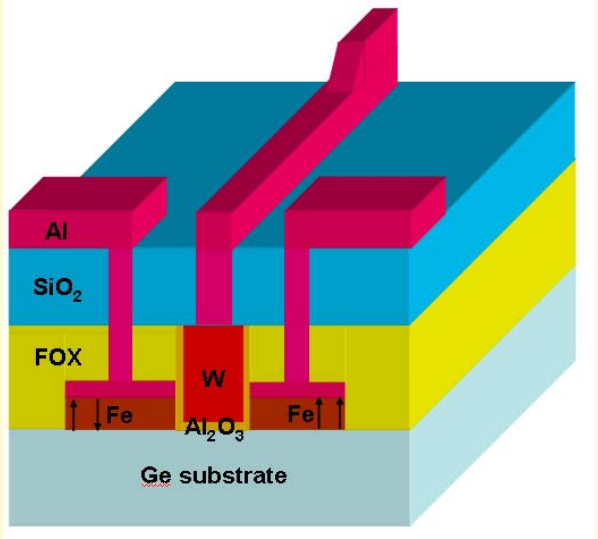


Field Effect in DMS Confirmed





Schematic Spin gain FET structure with a MnGe/SiGe quantum well.



Transistor with Memory

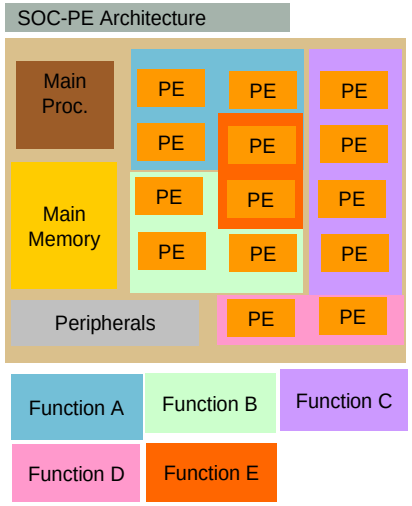
JingJing Chen and KL Wang et al., App. Phys. Letts. 90, 012501 2007

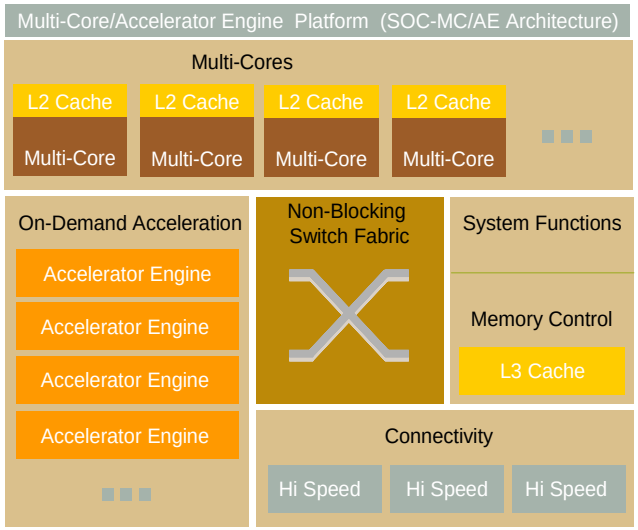
Supplementing CMOS

Basis of Existing Assessments of Logic Devices

General Purpose Processor

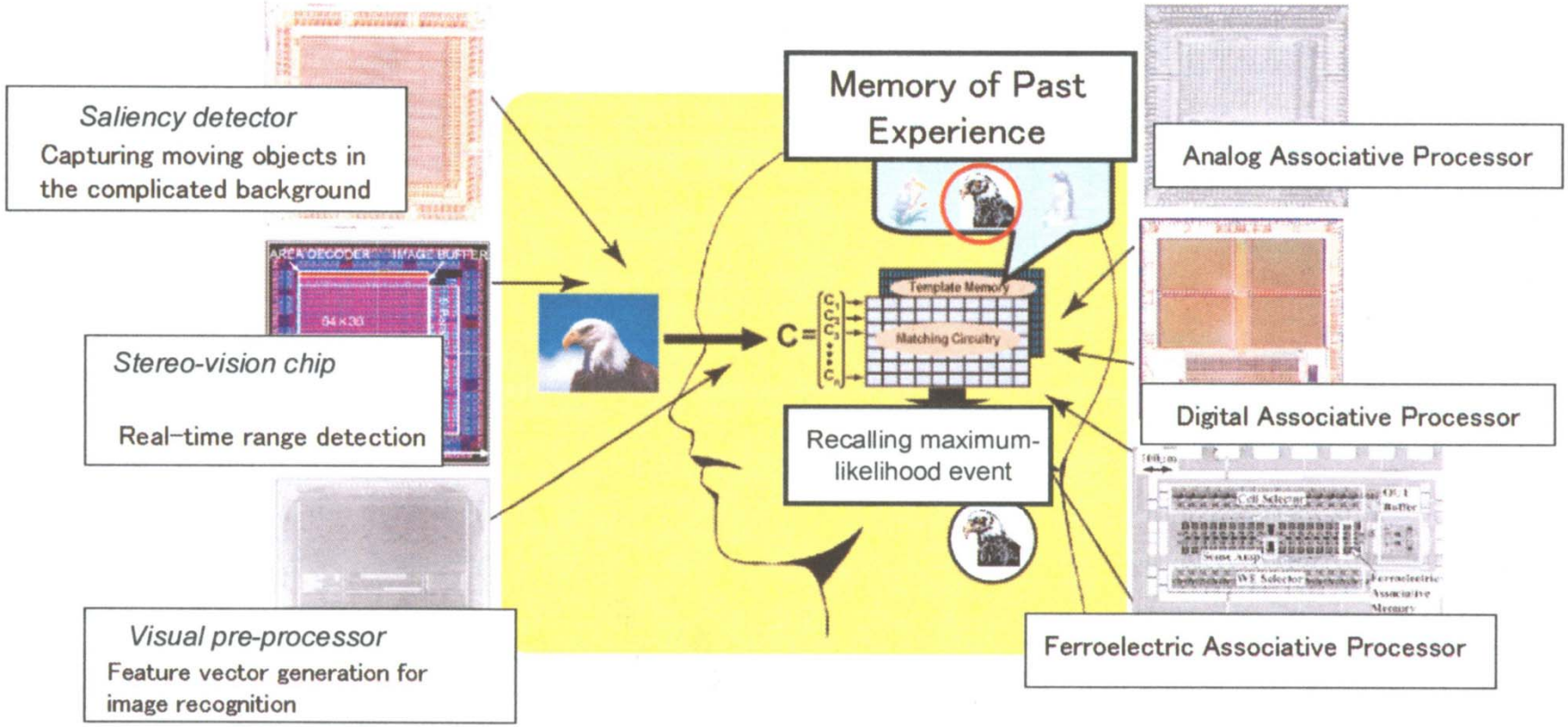
A possible ultimate evolution of **on-chip** architectures is Asynchronous ***Heterogeneous*** Multi-Core with Hierarchical Processors Organization





Courtesy Fawzi Behmann - Freescale

Top down information processing
Image Recognition



Tadashi Shibata, University of Tokyo

Image recognition

TABLE I
PERFORMANCES COMPARISON OF IMAGE RECOGNITION SYSTEMS

Search target: Sella (a pituitary gland)
Number of templates (generated by learning algorithm): 15
Search Area: 75x100-pel area

	Power(W)	Computational time (Second)	Total energy(J)
Pentium 4 1.5GHz Optimized in an assembly language level	54.7	5	273.5
Mobile Pentium 3 500MHz/1.1V Optimized in an assembly language level	3.5	15	52
Our digital vector generator & neural analog associative processor	0.152	1.2	0.182

Tadashi Shibata, University of Tokyo

Summary

- Geometrical and functional scaling is projected by the ITRS into the 2020's and likely beyond.
  - New MOSFET device structures are available
  - New "Channel Replacement" materials are being explored
  - Combinations of new materials & new structures are being investigated.
- Several new "Beyond CMOS" switching phenomena and "State Variables" are being pursued for new information processing approaches
  - No approach has been shown as a clear winner
  - Carbon-based Nanoelectronics has significant potential
- New markets requiring Functional Diversification will become important technology driver

CMOS vs. Nano:
No contest.

Steve Trimberger

Safe-Harbor Statement: This document contains forward-looking statements. Opinions expressed in this presentation are my own and do not necessarily represent the opinion of my employer or my employer's marketing department.

"Next week I plan to think about the option of using technology that isn't yet available."
- Wally in Dilbert 2007. Scott Adams

Engineering Fiction

Action	Science Fiction	Engineering Fiction
Cite a new effect or technology	Radiation induces mutation	Carbon nanotubes
Ignore limitations	Mutations can cause creatures to grow to enormous size	Scale up to manufacturability: quality, reproducibility
Postulate an infrastructure around it	Large creatures can survive unnoticed under the oceans	Nano fabrication facilities
Cite real, unimpeachable data	Dinosaurs had thick skin	Design a NAND gate from CNT switches
Tell fanciful stories	***Godzilla!***	***Nano-scale FPGA!***

Separating Fact From Fiction

XILINX.

Questions to the Panel

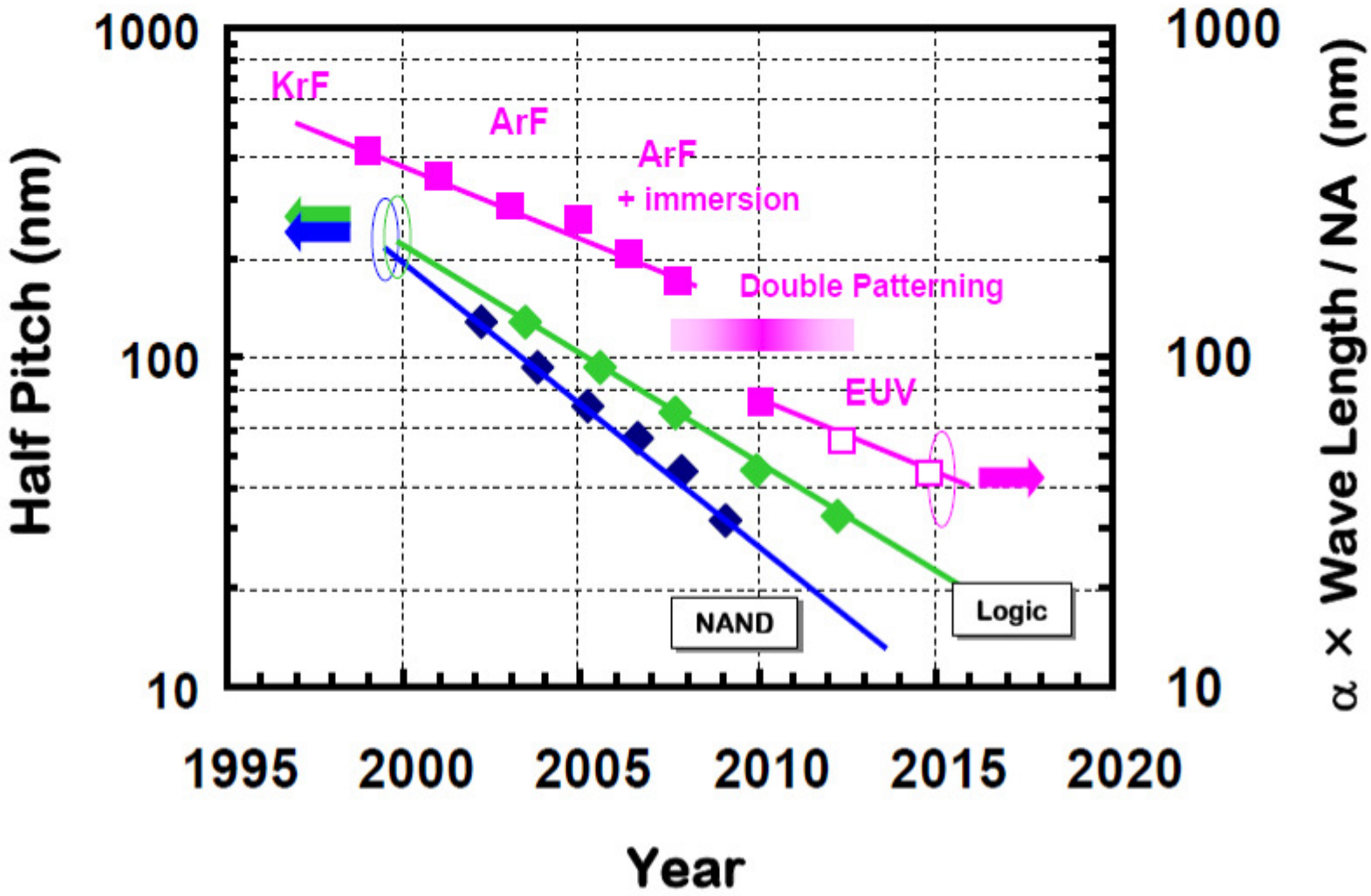
1) Do atomically-engineered materials and fabrication techniques offer new capabilities that are sufficiently compelling to encourage the necessary investment and learning?

- Yes, better is better.

2) What impact, if any, will bottom-up fabrication have--- augment lithographic processes, replace lithography, or remain a lab curiosity?

- Despite problems with optical lithography (see next slide), any displacing technology will need to give superior quality and reliability. You will know they're getting serious when they talk about purification techniques.

Lithography History & Future



Source: Nikon: http://www.nikonprecision.com/newsletter/summer_2008/toshiba_litho_2008.pdf

Questions to the Panel

1) Do atomically-engineered materials and fabrication techniques offer new capabilities that are sufficiently compelling to encourage the necessary investment and learning?
   - Yes, better is better.

2) What impact, if any, will bottom-up fabrication have—augment lithographic processes, replace lithography, or remain a lab curiosity?
   - Despite problems with optical lithography, any displacing technology will need to give superior quality and reliability. You will know they're getting serious when they talk about purification techniques.

3) What are the pros and cons of the CMOS/Nano hybrid solution?
   - Cost effective: only apply new technology where needed.

Questions to the Panel

4) How will FPGAs fare in this disruption (if any) compared to alternatives (ASICs, processors, multi/many-cores)? Will it upset the balance of power (Intel, Xilinx, Altera, HP, WindRiver, XtremeData, startups)?

- Fabrication technology won't change the balance of power, unless only one player can get it. Nano is so difficult that it is likely it requires the entire industry to produce it. Then all will have it.

5) Do nanoscale issues force architectural changes and paradigm shifts? What are the trends? Who will be impacted (FPGA designers, FPGA CAD, FPGA users)?

- Circuits may change. No change to the model is required. "We do Deep Sub-Micron design, so you don't have to" If necessary, we'll do Nano, so you don't have to.

6) Will FPGA vendors take the lead in this new paradigm and opportunity? Or, are they so risk-averse that they will leave it to startups?

- No. FPGA vendors are too smart to take the lead. Notice that they don't take the lead in process development or computer development today.

- **Nano might work**

- Nano might work someday.
- But we are WAY too early.
- And there's plenty to do right now that will benefit our customers.