Evening Panel

Programming High Performance Signal Processing Systems in High Level Languages

Chair: Kees Vissers (Xilinx)

Panelists: Devedas Varma (COO) AutoESL, Vinod Kathall (CTO) Synfora, Jeff Bier (CEO) BDTI, Don MacMillen (VP Software) Stretch, and Joseph Cavallaro (Professor) Rice University

Programming high performance signal processing systems is hard. Historically there has been a trade-off between ease of programming and absolute performance. It has long been understood that while for high-performance applications FPGAs are a great implementation technology, though historically they have come with a very poor programming model. For processor style architectures, such as DSPs, C-level languages are often used. Recently, there has been an emergence of C-level languages targeting FPGAs. In this panel we will discuss high level programming models and the efficiency of various technologies: DSP processors, C programming environments for FPGAs, and a completely integrated high level programming environment for a mixed technology. Both tool vendors and actual users will present the pros and cons.

Categories and Subject Descriptors: C.3 [Computer Systems Organization]: Special-Purpose and Application-based Systems

General Terms: Design, Performance, Languages

Keywords: FPGA, Signal Processing, DSP, High Level Programming Models

FPGA'10, February 21–23, 2010, Monterey, California, USA.
ACM 978-1-60558-911-4/10/02.